

**CHARACTERIZATION OF SELECTIVE EPITAXIAL GRAPHENE
GROWTH ON SILICON CARBIDE: LIMITATIONS AND
OPPORTUNITIES**

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The Academic Faculty

by

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Dedicated to the parents
of the little girl who evolved from learning her ABC
to the mature woman earning her PhD

Let my dissertation be a symbol of hope
for higher education for females everywhere

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SUMMARY

The need for post-CMOS nanoelectronics has led to the investigation of innovative device structures and materials. Graphene, a zero bandgap semiconductor with ballistic transport properties, has great potential to extend diversification and miniaturization beyond the limits of CMOS. The goal of this work is to study the growth of graphene on SiC using the novel method of selective graphitization. The major contributions of this research are as follows – First, epitaxial graphene is successfully grown on selected regions of SiC not capped by AlN deposited by molecular beam epitaxy. This contribution enables the formation of electronic-grade graphene in desired patterns without having to etch the graphene or expose it to any detrimental contact with external chemicals. Etching of AlN opens up windows to the SiC in desirable patterns for subsequent graphitization without leaving etch-residues (determined by XPS). Second, the impact of process parameters on the growth of graphene is investigated. Temperature, time, and argon pressure are the primary growth-conditions altered. A temperature of 1400°C in 1 mbar argon for 20 min produced the most optimal graphene growth without significant damage to the AlN capping-layer. Third, first-ever electronic transport measurements are achieved on the selective epitaxial graphene. Hall mobility of about 1550 cm²/Vs has been obtained to date. Finally, the critical limitations of the selective epitaxial graphene growth are enumerated. The advent of enhanced processing techniques that will overcome these limitations will create a multitude of opportunities for applications for graphene grown in this manner. It is envisaged to be a viable approach to fabrication of radio-frequency field-effect transistors.

CHAPTER 1

INTRODUCTION

1.1 Introduction

The minimum feature size used to fabricate integrated circuits (IC) has exponentially decreased thanks to the rapid pace of research and development. Moore's Law, the most frequently cited trend in the integration level, has accurately predicted the growth of computing power from the increasing density of transistor devices on IC chips since 1965 [1]. According to Moore's Law, the number of components per chip doubles roughly every 24 months [2]. The International Technology Roadmap for Semiconductors (ITRS) reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling, namely Moore's Law, has guided targets for over four decades, and will continue in many aspects of chip manufacture. However, CMOS scaling is facing significant challenges. Equivalent scaling, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this decade, and in the future. It is forecasted that by 2019 it will be necessary to augment the capabilities of the CMOS process by introducing new devices that will realize properties beyond those of CMOS devices [2]. Alternative state variables beyond charge state, such as spin state and molecular state, could usher in post-CMOS solutions beyond Moore's Law [3].

Figure 1.1 illustrates the incorporation into devices of functionalities that do not necessarily scale according to Moore's Law, but provide additional value to the end customer in different ways. This functional diversification typically allows for the non-

digital functionalities (such as RF communication, power control, passive components, sensors, actuators) to migrate from the system board level into a particular package-level (system-in-package, SiP) implementation [4]. Combined with the chip-level (system-on-chip, SoC) digital content, solutions beyond CMOS are envisioned.

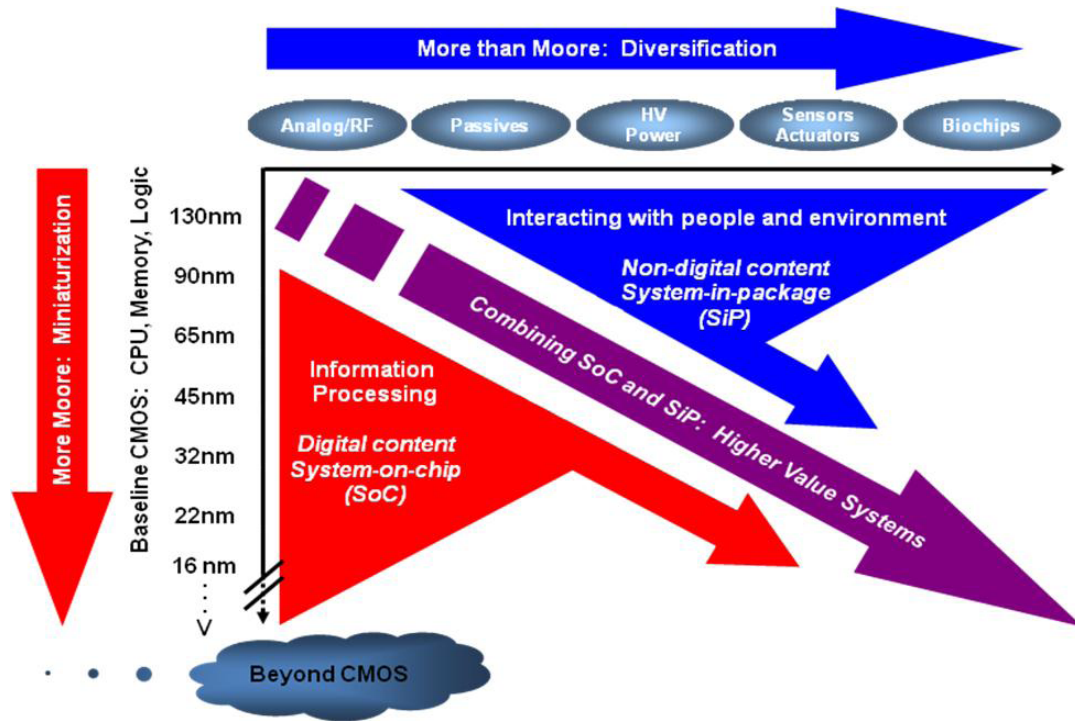


Figure 1.1: Beyond Moore's law [2].

With the industry going below 32 nm nodes, the competitiveness, functionality, and performance limits of CMOS and charge-based electronics are being questioned [3]. As the traditional MOSFET reaches nanoscale (feature size under 100 nm), several challenges arise [5] in the form of high electric fields, increased heat dissipation, interconnect delays, and leakage current. Some solutions to these problems have been realized with the implementation of new structures such as fully depleted silicon-on-insulator (FD-SOI) MOSFET and multiple-gate FET (such as finFET) [2]. New effects,

such as strain engineering, and the use of advanced materials, such as high-k dielectric and graphene, could also be considered for the diversification and miniaturization to go on beyond the limits of CMOS. In [4] the ITRS has introduced a new chapter on Emerging Research Materials to better reflect this evolution of the semiconductor industry. The novel material graphene is being investigated as a replacement for the ever-popular silicon as the channel material in transistors.

Graphene, a one-atom-thick layer of sp^2 – bonded carbon atoms arranged in a hexagonal pattern, shows outstanding electronic properties never before seen in materials. Epitaxial graphene, grown on a SiC substrate by the sublimation of Si atoms, is a promising method of producing large-surface area graphene films. Due to its compatibility with planar lithography processes, the cornerstone of current Si technology, epitaxial graphene is at the forefront of ushering in revolutionary carbon-based technologies, such as high radio-frequency field-effect transistors discussed later. All-graphene electronically coherent devices are also envisaged in the seminal paper by Dr. de Heer’s group [6].

The aim of this document is to fabricate and characterize patterned epitaxial graphene channels on silicon carbide via selective capping with AlN. The graphene is selective and epitaxial. This means the graphene is *epitaxially* formed by graphitization of C-face (000 $\bar{1}$) semi-insulating 4H-SiC by the sublimation of Si atoms from *selected* regions uncapped by aluminum nitride. The process of fabricating graphene Hall-bar structures is described, and the first-ever electronic transport measurements of selective graphene are performed. The effect of growth-conditions (temperature, time, and background argon pressure) on selective graphitization is detailed, along with critical limitations and potential applications of the process.

1.2 Background

1.2.1 Silicon MOSFET

The conventional MOSFET (Metal Oxide Semiconductor Field Effect Transistor) consists of the source, channel, and drain, and a nearby gate separated from the channel with a barrier (gate dielectric). The input terminal voltage (voltage between the gate and the source) modulates the electron density of the channel and controls the flow of current between the other two terminals (source and drain). The Field Effect Transistor (FET) is so called since the electric field applied to the input terminal is what affects the flow of current between the other two terminals. This property allows a transistor to operate as a switch [7]. Figure 1.2 shows the cross-sectional view of an n-channel MOSFET.

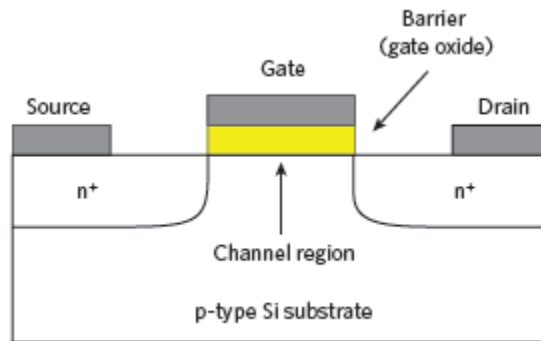


Figure 1.2: Cross sectional view of n-channel MOSFET.

Electrical current can flow from the source to the drain depending on the charge applied to the gate region. In Si MOSFETs until the introduction of the 45 nm node in 2007, the gate electrode used to be a layer of polysilicon, placed over the channel but separated from the channel by a thin insulating layer (traditionally SiO_2). The semiconductor material in the source and drain regions is doped with a different type of material than in the region under the gate, so an NPN or PNP type structure exists

between the source and drain regions of a MOSFET. If it is an n-channel MOSFET (NMOS) the drain and source are of n-type material and the main body is of p-type material. If it is a p-channel MOSFET (PMOS) then the drain and source are of a p-type material. When a voltage is applied between the gate and source terminals, the electric field generated penetrates the oxide and creates an “inversion layer” below the oxide. The inversion layer is of the same type (P-type or N-type), as the source and drain, so that layer provides a channel through which current can pass.

The voltage between the gate and the source, V_{GS} , and the voltage between the drain and the source, V_{DS} , are primary parameters determining the transistor behavior. Another vital parameter is the threshold voltage V_T which is specific for each individual transistor. It depends on the gate and substrate doping, and determines the voltage level at which the transistor turns on. When a voltage that is greater than the threshold voltage is applied to the gate, a conducting channel is formed between the drain and source. For an NMOS, the threshold voltage is positive, which attracts electrons towards the gate leading to inversion and formation of the n-channel between the source and drain. On the other hand, for a PMOS, the threshold voltage is negative, which repels electrons away from the gate leading to inversion and formation of the p-channel between the source and drain.

Si MOSFETs have undergone massive scaling to keep up with Moore’s Law. As of 2007, the polysilicon gate has been replaced by a metal gate, while the gate dielectric is high-k (typically hafnium-based oxide). There are several advantages to the reduction in size. A smaller MOSFET has a smaller gate and thus lower gate capacitance. These two factors allow for shorter switching time and higher processing speed. Yet another

benefit of a smaller MOSFET is the fact that it can be packed more densely resulting in chips with more computing power in the same area. Until the late 1990s, this size reduction resulted in great improvements to the operation of the MOSFETs without any negative consequences. Of late, further size reduction has given rise to operational problems, as discussed below.

- Small MOSFET geometries require small values for the threshold and gate voltages to maintain performance and reliability. With reduced threshold voltage, the transistor cannot be completely turned off, resulting in a weak-inversion layer that consumes power in the form of subthreshold leakage. Subthreshold leakage, which was negligible in the past, can now consume up to half of the total chip power in the form of heat [8].
- At high temperatures, circuits have shorter lifetimes and reduced reliability. Heat-sinks and other cooling methods are required for many ICs including microprocessors. When the heat-sink is unsuccessful in keeping the temperature low enough, the on-state resistance rises with temperature. The resultant dissipated power generates further heat, raising the junction temperature quickly and uncontrollably, possibly destroying the device [9, 10].
- Switching time is roughly proportional to the gate capacitance. However, with transistors becoming smaller and more transistors being placed on the chip, the interconnect capacitance (the capacitance of the wires connecting different parts of the chip) contributes significantly to the total capacitance. Signals

have to travel through the interconnects, which leads to increased delay and lower performance [11].

- Furthermore, as the contact becomes thin, the high current density causes electromigration. Under the influence of current, individual atoms can be displaced from the metal lattice and migrate in the direction of the carriers flowing. This results in piling up of metal at the positive electrode end and depletion at the negative end. This process of electromigration ultimately results in contact failure [12].

The 22 nm node is the current CMOS technology node. Intel announced the world's first 22 nm 3D transistor in 2011. By 2026, silicon MOSFETs will face immense challenges in how short engineers can make a channel and gate and how thin a gate insulator they can support [2].

1.2.2 Graphene FET

The promising new semiconductor material –graphene – hopes to overcome the limits of silicon. Two major types of graphene exist depending on how they are produced – exfoliated and epitaxial. Exfoliated graphene is mechanically extracted from bulk graphite crystals onto a SiO_2/Si substrate [13, 14]. Epitaxial graphene is grown on a SiC substrate by the sublimation of Si atoms [15, 16].

Graphene (epitaxial and exfoliated) shows novel electronic properties never exhibited before. It is a zero band-gap semiconductor, with a band structure as shown in Figure 1.3. The conductance band touches the valence band at the Dirac point.

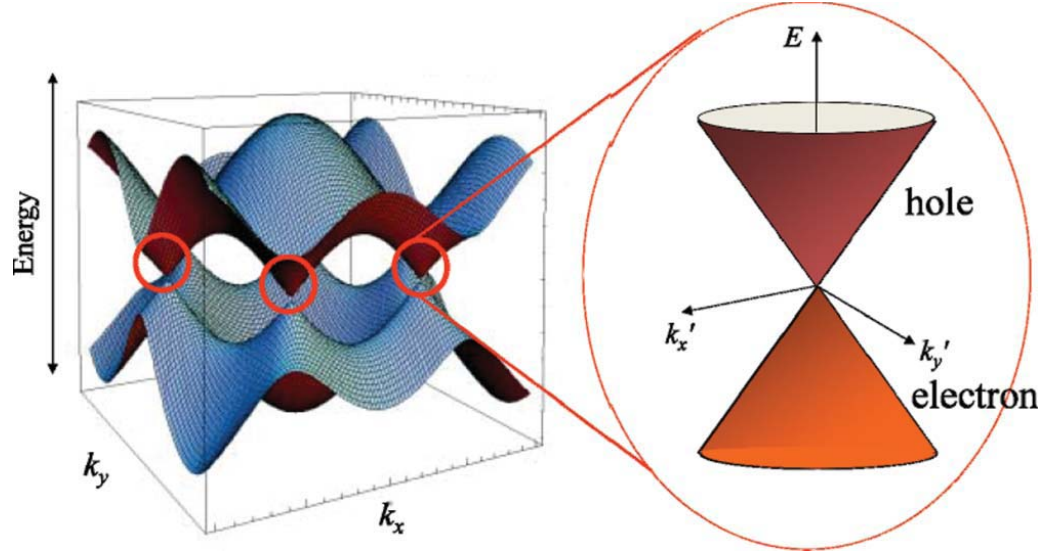


Figure 1.3: Band structure of graphene: electron energy versus wave-vector dispersion [17].

Electrons in graphene, obeying a linear dispersion relation, behave like massless relativistic particles (Dirac fermions), described by the energy equation, $E(k) = \hbar k v_F$, where $\hbar k$ is the momentum and v_F is the Fermi velocity [18]. Although there is nothing particularly relativistic about electrons moving around carbon atoms, their interaction with the periodic potential of graphene's honeycomb lattice gives rise to new quasiparticles. The speed of these quasiparticles is independent of their energy, and at low energies exhibits a Fermi velocity of 10^6 ms^{-1} accurately described by the (2+1)-dimensional Dirac equation [19]. These Dirac fermions can be seen as electrons that have lost their rest mass m_0 or as neutrinos that acquired the electron charge e that move through graphene as waves, rather than particles. Graphene is coherent, meaning electrons move through the graphene much like light travels through waveguides. Such nanometer-scale devices that manipulate electrons as waves have no analog in silicon-based electronics. The relativistic-like description of electron waves on honeycomb lattices has been known theoretically for many years. The experimental discovery of

graphene provides a way to probe quantum electrodynamics (QED) phenomena by measuring the electronic properties of graphene.

Graphene has high electron mobility, implying electrons move through it without much scattering or resistance. Mobilities of $\sim 20000 \text{ cm}^2/\text{Vs}$ are easily achieved at the current state of graphene technology, which is already an order of magnitude higher than the literature data of ultra-thin body silicon-on-insulator (SOI) devices [20]. The electrons also possess the properties of Dirac particles, which allow them to travel significant distances without scattering. Dirac particle properties include an anomalous Berry's phase of π , weak anti-localization and square root field dependence of the Landau level energies[14, 21]. Unusual electronic properties, such as anomalous Quantum Hall Effect and absence of Anderson localization, are observed in a Dirac fermion system like graphene [18]. In addition to the 2D confinement in the plane of graphene, the graphene electrons (or holes) can be further confined by forming narrow ribbons, thus opening a transport gap in the band structure. The energy gap that opens up is found to be inversely proportional to the ribbon width [22].

Along with the excellent electronic properties, graphene has outstanding mechanical and thermal properties. It is a stable material down to true nanometer sizes [19]. It has great tensile strength and elastic properties. Graphene exhibits a breaking strength of $\sim 40 \text{ N/m}$, reaching the theoretical limit. Record values of thermal conductivity at room temperature ($\sim 5000 \text{ W m}^{-1} \text{ K}^{-1}$) and Young's modulus ($\sim 1 \text{ TPa}$) are also reported [23].

Most graphene FETs have been demonstrated using exfoliated graphene flakes on top of a SiO_2 layer over silicon wafer [20, 24, 25]. The graphene films are prepared by

mechanical exfoliation (repeated peeling by adhesive tape) of small mesas of highly oriented pyrolytic graphite (HOPG). Few-layer graphene (FLG) films up to 10 μm in size are obtained on top of a silicon substrate with 300 nm of silicon dioxide (SiO_2). Silicon oxide (SiO_x) is commonly used as the top-gate dielectric. Metal (typically Cr/Au) is used as source, drain, and top-gate electrodes, while the silicon substrate is used as the back-gate. Few- and monolayer graphene has been investigated with respect to its application in field-effect devices for nanoelectronics. The top-gate with SiO_2 dielectric reduces electron and hole mobility compared to pseudo-MOS structures with only the back-gate. Despite the limiting effect of the top-gate electrode, carrier mobilities of 10000-15000 cm^2/Vs are routinely measured for such transistors [26]. Graphene exhibits the highest carrier (electron and hole) mobility ($10^5 \text{ cm}^2/\text{Vs}$) at room temperature [27]. This is not only ~ 100 times greater than that of Si but also about 10 times greater than the state-of-the-art semiconductors lattice-matched to InP, currently regarded as the best high-speed materials [27]. Hall mobility of graphene channels is measured to be higher than FET mobilities. Upon gating the FET, trapped charge or interface charge in the gate-dielectric layer can lead to a reduction in the transconductance and the mobility.

Epitaxial graphene grown by the graphitization of SiC substrates has also been implemented in graphene FETs [28]. The electric-field effect has been observed on epitaxial graphene multilayers grown on SiC substrates by thermal decomposition of SiC. Carrier mobilities up to $2.5 \times 10^4 \text{ cm}^2/\text{Vs}$ have been measured. Both side-gated and top-gated graphene FETs have been fabricated using standard semiconductor processes on both the Si- and the C-face of the SiC substrates [29]. At the gate-voltage corresponding to the maximum source-drain resistance, the Hall voltage changes sign indicating a

transition from hole- to electron-carried transport, consistent with the graphene band structure. These results indicate the potential of epitaxial graphene as a platform for large-scale graphene-based electronics [30, 31].

The graphene FET is essentially ambipolar, meaning the transport is dominated by electrons (for positive gate-voltages) and holes (for negative gate-voltages). The conductance minimum of the $I_D - V_G$ curve where electrons and holes make equal contributions to the transport is known as the Dirac point. Although the density of states (DOS) at the Dirac point is zero, a minimum conductivity on the order of e^2/h is found experimentally for graphene when the Fermi level is aligned with it [32]. The limited I_{on}/I_{off} ratio of graphene FETs may inhibit their application in computer logic, but RF applications hold promise. The 2D nature of graphene has a distinct advantage in that the drive current of the RF FET, in principle, can be scaled up by increasing the device channel width [33]. Graphene, the thinnest electronic material, has very high carrier mobilities enabling transistors operating at very high frequencies. Epitaxial graphene can be selectively grown in desired regions of the SiC substrate [34], generating electronic-grade films essentially untouched by external chemicals that may degrade graphene performance. Such selective epitaxial graphitization produces high-mobility films that can be patterned by conventional lithographic processes to fabricate RF FETs. In the epitaxial graphene RF FET demonstrated in [27], the low-field FET mobility reduced to $\sim 200 \text{ cm}^2/\text{Vs}$ from the original carrier mobility of $1000 \text{ cm}^2/\text{Vs}$, leading to a cutoff frequency of 4.4 GHz. This reduction is also seen in [33] where the mobility reduced to $400 \text{ cm}^2/\text{Vs}$ after deposition of the top-gate dielectric, generating a cutoff frequency of 26 GHz. The latest graphene RF FETs report a maximum extrapolated cutoff frequency of 100 GHz [35] with an electron carrier density of $\sim 3 \times 10^{12} \text{ cm}^{-2}$ and a Hall mobility between 1000 to $1500 \text{ cm}^2/\text{Vs}$.

1.3 Motivation

Not only does epitaxial graphene demonstrate exceptional mobility values ($> 10^4$ cm²/Vs), but also it exhibits the following advantages:

- **Lithographic patternability:**

Channel, source, and drain regions formed by a single patterning step, requiring only the addition of the gate-stack and contacts to complete the transistor. The planar lithography process, the cornerstone of current Si technology, is compatible with graphene processing.

- **Tunability of electronic properties:**

Metallic versus semiconducting graphene nano-ribbon (GNR) can be selected by the orientation of the edge-termination. A zigzag crystallographic-direction of the ribbon-axis indicates metallic properties. An armchair direction indicates either metallic or semiconducting properties [6, 36].

- **Band-gap engineering:**

The GNR width determines the band-gap of graphene. The band-gap (or pseudo band-gap) varies approximately as the inverse of the width [22].

- **Seamless device integration:**

Functional graphene devices can be fabricated eliminating the need for metal interconnects and contacts on the wafer. These components can themselves be made of graphene, eliminating the interface between different materials. An armchair ribbon of 10 nm width is generally semiconducting, while a zigzag ribbon of 100 nm width is metallic at room temperature [6, 36]. This seamless

device integration not only makes integration of structures simpler, but also ensures their long-term integrity.

This work characterizes the growth of selective epitaxial graphene in an argon-environment. Graphene is selectively grown in desired regions of the SiC substrate [37]. This creates graphene in the pattern desired, and also eliminates extraneous contact with etchants that may degrade the graphene quality. The performance of graphene devices is highly dependent on sample preparation; hence it is critical to control the environment of graphene [38]. Electron-beam lithography, typically used in the fabrication of graphene nanostructures, exposes the graphene to e-beam resist, which can leave behind contaminants that may modify its electronic transport properties [39]. Also, dry etching in oxygen plasma, commonly performed to obtain graphene nano-ribbons, introduces dangling bonds and defects at the edges of the ribbons, decreasing the carrier mobility [40]. Furthermore, wet etching of graphene causes unintentional doping of the graphene layer, altering the device performance [41].

To address the issue of degradation in performance, annealing in UHV or Ar/H₂ atmospheres has been studied by scanning tunneling microscopy (STM) [38, 42]. Also, current-induced annealing has been performed in a cryostat to reduce contamination [41]. More recently, an aluminum nitride (AlN) capping layer has been utilized for selective growth of graphene in non-capped areas, providing a bottom-up approach to fabricating patterned graphene structures [37]. AlN has been employed for some time to obstruct Si sublimation during high-temperature annealing to activate ion-implanted dopants in SiC [43]. The AlN films are believed to withstand temperatures up to 1600°C without significant damage [44], thereby showing great potential to form an effective capping

layer against graphitization at high temperatures, and enabling the formation of electronic-mobility graphene.

C-face (000 $\bar{1}$) multilayer graphene has domain sizes much larger than those grown on the Si-face (0001). The improved structural order of C-face films correlates with magnetotransport measurements showing an order of magnitude improvement in electron mobilities over Si-face films [45]. Also, electronic coherence lengths exceeding 1 μm have been measured for multilayer graphene films prepared on the C-terminated face of SiC [6]. Furthermore, improved morphologies are observed on C-face films grown under argon as compared to high vacuum. Carrier mobilities increase and sheet carrier densities decrease through argon-assisted growth, possibly due to reduced scattering in the films [46]. These high-mobility films can be patterned via conventional lithographic techniques enabling the integration of graphene into nanoelectronic device structures.

1.4 Organization

The rest of the dissertation is organized as follows. In Chapter 2, the fabrication-process for selective graphitization is described. Using aluminum nitride as a capping layer, graphene is selectively grown in desired regions of SiC. The impact of process parameters, such as temperature, time, and argon pressure, on the growth of graphene is discussed. Chapter 3 describes two methods for the fabrication of graphene Hall-bar structures. The first method uses e-beam lithography to pattern the structure, and removes the AlN by wet-etching. The more improved method uses photolithography and dry-etching. Results from electronic transport studies performed on both are listed.

Chapter 4 enumerates critical limitations of the selective epitaxial graphene growth technique, with recommendations for improvement. In Chapter 5, the opportunities for potential applications of graphene thus grown are explored.

The fabrication of nano-scale gaps using e-beam lithography is discussed in Chapter 6. The generation of sub-10 nm gaps with good repeatability enables possible applications in single-molecule detection and molecular electronics. Chapter 7 presents conclusions and recommendations for future work.

CHAPTER 2

SELECTIVE EPITAXIAL GRAPHENE

2.1 Introduction

Graphene, a two-dimensional hexagonal network of sp^2 -bonded carbon atoms with outstanding electronic transport properties, is a promising candidate for post-CMOS solutions. Epitaxial growth of graphene by induction-furnace heating of monocrystalline SiC to above 1200°C and subsequent Si sublimation is the best method for producing large surface-area graphene films [6, 15, 16]. These high-mobility films can be patterned via conventional lithographic techniques enabling the integration of graphene into nano-electronic device structures potentially supplanting silicon.

Although graphene has heralded intensive research, the study of selective growth of graphene has been limited so far. This chapter discusses graphene grown using this novel technique. Electronic-quality epitaxial graphene was selectively grown on silicon carbide in regions not masked by an aluminum nitride capping layer. Patterning of the cap exposes SiC where graphene will grow, providing a pathway to produce device structures that avoid lithographic patterning of graphene itself. The impact on graphene-growth of different process parameters is also investigated. Analysis of both C-face and Si-face of SiC is detailed, and the optimal growth-conditions are established. Capped areas greatly inhibit graphene growth at the graphitization temperature of 1400°C under argon pressure of 100 Pa. The graphene was characterized by scanning probe microscopy and Raman spectroscopy.

AlN has been employed for some time to prevent Si sublimation during high-temperature annealing for activation of ion-implanted dopants in SiC [43]. AlN has the ability to withstand temperatures up to 1600°C without significant damage [44]. It also shows great lattice and thermal match to the SiC substrate. A host of techniques exist for AlN deposition – RF sputtering [47], pulsed-laser deposition (PLD) [44], metal organic chemical vapor deposition (MOCVD) [48], atomic-layer deposition (ALD) [49], and molecular beam epitaxy (MBE) [50], just to name a few. For the purposes of capping for selective graphitization, the MBE process proved to be successful. The crystalline nature of the AlN formed by MBE was hugely successful in preventing Si atoms from sublimating from the SiC surface due to the non-porous nature of the capping layer. For MBE AlN conducted for this research, a deposition pressure of E-5 Torr was used, which led to good coverage of the AlN, hence making it an effective encapsulant for subsequent selective graphitization.

The method of growing graphene on SiC described in this chapter suitably eliminates any unnecessary contact with external chemicals. The AlN acts as a capping layer to prevent graphene from forming by Si sublimation in the unexposed areas under it. By patterning and etching AlN to open up windows on the SiC surface for subsequent graphitization, the resulting graphene is essentially untouched by any extraneous matter, producing electronic quality material. Though the SiC surface comes in contact with the etchants, AFM shows negligible surface roughness and XPS shows undetectable residue-levels.

2.2 Process-Flow for Fabrication of Selective Epitaxial Graphene

The process-flow for selective graphitization as a method for producing electronic-quality graphene is described in detail below, and illustrated in Appendix A. After several process iterations, the following is the final established fabrication-process:

1. **SiC Substrate Preparation:** *This process cleans the SiC sample in preparation for subsequent processing*
 - Sonication (10 min in acetone and 10 min in isopropyl alcohol)
 - Roughen back-side (Si-face) with Plasmatherm SLR RIE system
 - Deposit 1 μm tantalum (Ta) on the rough side using Unifilm Sputterer (SiC substrate is transparent and requires backside metallization before MBE to promote thermal absorption)
 - Sonication (as before)
2. **Hydrogen Etching:** *This process smoothens the C-face of SiC surface (detailed in Appendix B)*
3. **AlN Deposition:** *This process deposits aluminum nitride that acts as the capping layer against graphitization (detailed in Section 2.3)*
 - HF 30 s dip (removes any oxides from SiC surface)
 - Deposit AlN with optimal Al-flux during MBE (based on RHEED)
4. **SiO₂ Deposition:** *This process deposits silicon dioxide as an etch mask for aluminum nitride*
 - Run clean recipe on Plasma Enhanced Chemical Vapor Deposition (PECVD) system
 - Deposit $\sim 1 \mu\text{m}$ SiO₂:
Temperature: 300 °C, SiH₄ flow-rate: 400 sccm, N₂O flow-rate: 900 sccm, Pressure: 900 mTorr, RF power: 25 W, Deposition rate: $\sim 50 \text{ nm/min}$
5. **Patterning:** *This process performs photolithography to pattern the Hall-bar structures on SiC surface for subsequent mobility measurements*
 - Photolithography:
1.3 μm Shipley 1813 positive photo-resist spun on sample: 1000 rpm for 30 s
 - Soft bake: 95°C for 90 s
 - Exposure energy: 120 mJ/cm² (lamp intensity measured with 365 nm)

- detector to determine exposure time)
 - Develop: MF 319 for 30 s with slight agitation
 - DI water rinse
- 6. Etching:** *This process removes the mask materials (silicon dioxide and aluminum nitride) from desired regions exposing the silicon carbide surface for subsequent graphitization*
- Run clean recipe on Inductively Coupled Plasma (ICP) etch-system
 - SiO₂ etch (resist as etch mask):
Ar: 15 sccm, O₂: 3 sccm, CF₄: 10 sccm, C₄F₆: 10 sccm, Coil power: 400 W, Platen power: 100 W, Etch rate: ~ 50 nm/min
 - AlN etch (SiO₂ as etch mask):
Cl₂: 32 sccm, BCl₃: 4 sccm, Ar: 5 sccm, Coil power: 500 W, Platen power: 70 W, Pressure: 5 mTorr, Etch rate: ~ 80 nm/min
- 7. Surface Cleaning:** *This process cleans unwanted deposits from the sample in preparation for graphitization at high temperatures*
- Remove resist (with acetone)
 - Remove metal from back-side (with hydrofluoric acid)
- 8. Graphitization:** *This process grows electronic-quality graphene on SiC*
- Temperature: 1400°C, Ar pressure: 1 mbar, Time: 20 min
- 9. Electronic Transport:** *This performs Hall-bar measurements on graphene (detailed in Chapter 3)*
- Carrier density, sheet resistance, and mobility values obtained

Research-grade undoped semi-insulating single-crystal 4H-SiC wafer was obtained from Cree, Inc. in Durham, NC. The wafer thickness was 366 μm with an orientation of 0.03° . The wafer was diced into 1 cm^2 samples in preparation for AlN deposition by MBE. Prior to deposition, the surface of the sample was cleaned by sonication (in acetone and isopropyl alcohol), flattened by H₂ etching (1500°C for 30 min), and oxide-stripped (30 s dip in 10% hydrofluoric acid). The sample then underwent MBE on the C-terminated (000 $\bar{1}$) face of SiC at 700°C under a pressure of 1.5E-5 Torr

and power of 350 W. The aluminum flux was shuttered at a rate of 0.1 Hz while the nitrogen flux was constant at 1.3 sccm (standard cubic centimeters per minute, used to quantify gas flow) to produce an AlN film of thickness approximately 80 nm. Hall-bar structures for subsequent transport measurements were then patterned on the sample.

The exposed SiC regions (without AlN capping), formed after etching the mask materials (SiO₂ and AlN), were then graphitized to form graphene Hall-bar structures. The graphene growth consisted of three steps – first, 10 min at 200°C in vacuum (~E-8 Torr) to desorb moisture from the sample; second, 20 min at 1200°C to remove any oxides from the exposed SiC surface and to flatten the surface by SiC step-flow; and finally, 20 min at 1400°C in a background pressure of 100 Pa (~0.75 Torr or 1 mbar) of Ar. Following graphitization, the sample was cooled down gradually to 600°C at the rate of 50°C/min.

Patterning and etching AlN opened up windows on the SiC surface for graphitization. The resulting graphene is essentially untouched by any extraneous matter, apart from etching residues (if any) that were not completely removed during etching (see Figure 3.1). This process produces electronic quality material. The prepared surface was graphitized in two different environments – under high vacuum and under Ar pressure. Each of these steps is described in depth in the following sections.

Method 1: Under High Vacuum

Graphene growth consisted of a first step at 200°C for 10min in vacuum (~E-8 Torr) to desorb moisture from the sample followed by heating the sample up to 1200°C for 20 min to remove any oxides from the exposed SiC surface and to flatten the surface by SiC step-flow. Finally graphene was grown at 1400°C for up to 10 min under vacuum.

Method 2: Under Ar Pressure

Graphene growth consisted of a first step at 200°C for 10 min in vacuum ($\sim 10^{-8}$ Torr) to desorb moisture from the sample followed by the introduction of 100 Pa of argon. Then, the sample was heated up to 1200°C for 20min to remove any oxides from the exposed SiC surface and to flatten the surface by SiC step-flow. Finally graphene was grown at 1400°C for 20min in the argon-environment. The presence of argon during growth slows down the rate of graphene formation on the C-face [51], hence the time was increased by 10 min from the high vacuum growth.

2.3 Aluminum Nitride as Graphitization Mask

Since the 1920s, AlN has been studied for its outstanding properties, including high thermal conductivity, hardness, piezoelectricity, chemical resistance, temperature resistance, wide band-gap, and lattice and thermal expansion matching to substrates such as sapphire and silicon [50].

In this experiment, AlN is being used as a capping layer for subsequent epitaxial graphitization of SiC due to its high temperature resistance [52] and its lattice and thermal expansion matching to the SiC substrate [53, 54]. Research-grade semi-insulating single-crystal 4H-SiC was used for all experiments. Prior to AlN deposition on the C-face, the surface of the SiC sample was cleaned by sonication (in acetone and isopropyl alcohol), flattened by H₂ etching (1500°C for 30 min), and oxide-stripped (30s dip in 10% hydrofluoric acid). To ensure that these processing steps do not contaminate or damage the SiC wafer, AFM imaging is performed after each step to analyze surface quality. The aluminum nitride was deposited by molecular beam epitaxy (MBE).

The MBE system (operated by Dr. Doolittle's research group) was used for the deposition of the AlN. Further details about this system can be found in Appendix C. In the introduction-chamber of the system, a 30 min outgassing at 250°C was performed prior to the MBE process. The AlN deposition process parameters are provided in Table 2.1.

Table 2.1: MBE process parameters.

Substrate	4H-SiC (C-face)
Substrate Temperature (°C)	700
Substrate to Target Distance (in.)	12
Target	Aluminum (99.999% pure)
Beam Equivalent Pressure, BEP_{Al} (Torr)	4.63E-7
Temperature, T_{Al} (°C)	1135
RF Power (W)	350
Process Pressure (Torr)	1.5E-5
Aluminum Shutter Modulation	10 s open, 10 s closed
Nitrogen (99.999%) Flux	1.3 sccm, always open
Time (min)	6
Thickness (nm)	80
Deposition Rate (nm/min)	~13

The MBE used the metal modulation epitaxy process (MME), along with reflection high-energy electron diffraction (RHEED) exposure, on the rotating SiC

sample. The MME process utilizes a shutter modulation growth technique [50, 55]. The films grown using MME when compared to films grown with no shutter modulation show much improved surface roughness determined by atomic force microscopy. For the same Al flux that resulted in droplets with the unmodulated sample, the MME sample exhibits no droplets, and the surface roughness reduces by half, from 6.92 nm to 3.29 nm. By using MME, a wider range of Al flux is allowed for Al-rich growths without droplets [50].

The repeatable characteristics of the RHEED intensity upon shutter transients can be used to determine growth conditions in situ. It was observed that the time constant of the falling RHEED intensity upon shutter opening was inversely correlated with the Al flux and that the time constant was repeatable to very high accuracy [56]. The MME process, along with RHEED signatures, can therefore be used to obtain repeatable growth conditions. This growth technique has shown improved morphology of AlN due to the increased adatom migration and improved lateral growth.

The XRD rocking curve of an MBE grown AlN sample shows the crystalline nature of the AlN obtained by this process. The $\langle 002 \rangle$ orientation of AlN is observed, as shown in Figure 2.1.

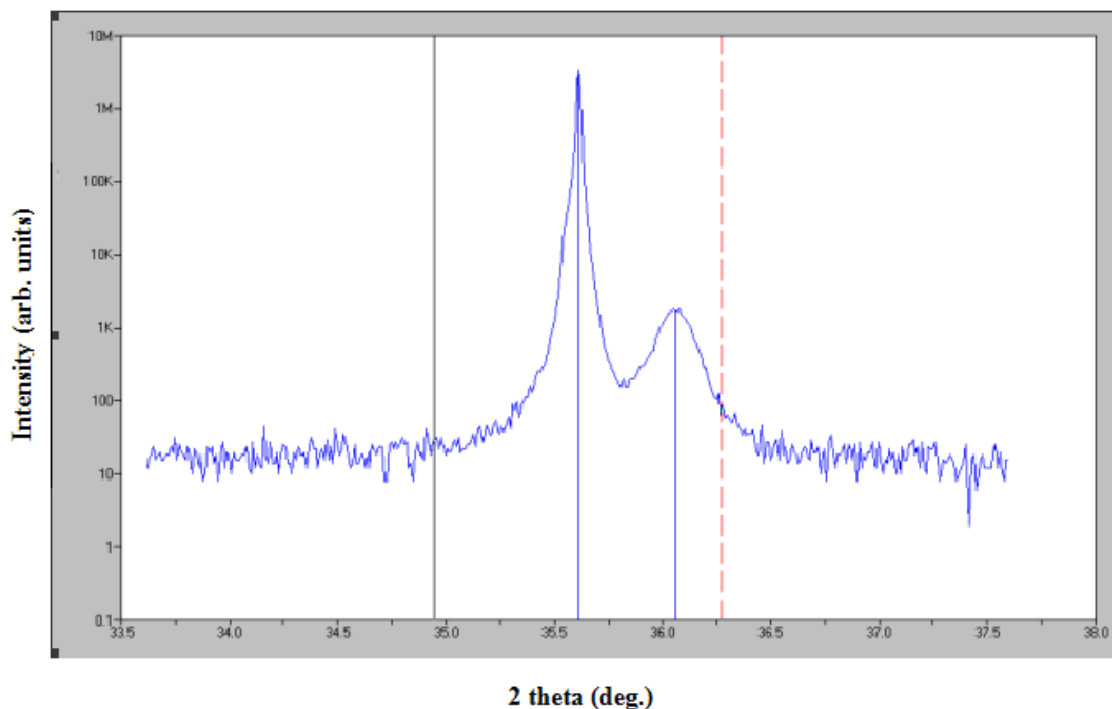
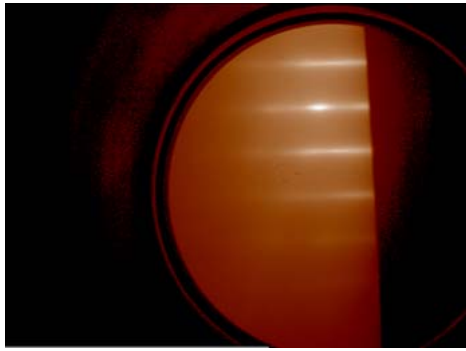
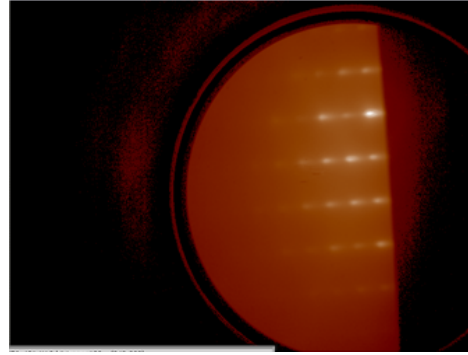


Figure 2.1: XRD rocking curve of MBE AlN. SiC peak is seen at 35.6° . AlN peak corresponding to the $\langle 002 \rangle$ orientation appears around 36° .

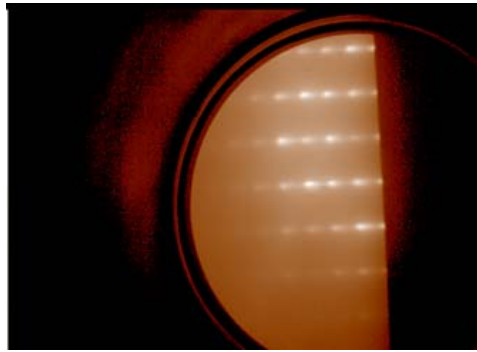
The RHEED patterns obtained on the sample while it underwent MBE can be seen in Figure 2.2. From the RHEED intensity in Figure 2.2-c, it is observed that there is some build-up of N in the AlN film as indicated by the spots within the streak in the RHEED pattern. This issue can be resolved by growing the AlN in an Al-rich environment. It is believed that optimization of the Al flux (as determined by the RHEED pattern) for the purpose of high-quality crystalline growth of AlN improved the morphology of AlN in later runs. This in turn made it even more effective in capping against graphitization.



a) SiC substrate



b) During AlN growth



c) End of growth

Figure 2.2: RHEED patterns obtained in situ on the SiC sample during different phases of the MBE of AlN. The microscope used a 50x lens.

Topographical characterization of the sample surface was carried out on an atomic force microscope (Digital Instruments CP-II AFM) in non-contact mode. The SiC terraces - both before and after the MBE process – look identical, suggesting insignificant step-flow of SiC during AlN growth. Due to SiC being IR-transparent, the back-side is roughened and metalized so that the sample heats up to the desired temperatures during MBE.

2.4 Characterization of Epitaxial Graphene Growth on C-Face and Si-Face

The process of selective graphitization was performed on the C-face ($000\bar{1}$) of SiC. Temperature, time, and argon pressure were the primary process parameters that were altered. In the initial experiments, argon was introduced into the graphitization chamber at 200°C. The chamber was then heated up to the desired graphitization temperature in the argon environment. It was noted that under these conditions, the thermocouple did not register the proper temperature of the chamber. Since a lower temperature was measured than actual, the power supply ramped up to a much higher power (> 10000 W) than needed to compensate for the low-temperature reading. This led to over-heating of the sample, and degradation of the AlN coating.

In subsequent experiments, argon was therefore introduced at a higher temperature of 1200°C. This led to the proper reading of temperature using the thermocouple, and the power supply ramped up to about 8000 W.

Table 2.2 summarizes the results from heating a patterned SiC sample with AlN capping layer on top. Argon pressure, temperature and time were the variable process parameters. The table shows how the sample behaves – whether the SiC graphitizes, and whether the AlN sustains the high growth temperatures. For Sample # 6, the graphene-growth criterion was inconclusive. This means that some samples showed graphene, while others did not under the same growth-conditions. As for Sample # 13, no conclusive data for either behavior was observed.

Table 2.2: Table summarizing the behavior of graphene growth in different processing conditions.

C-face	Growth Conditions			Does graphene grow?	Does AlN sustain growth?
Sample #	Temperature (°C)	Time (min)	Argon Pressure (mbar)		
1	1400	20	0	Yes	No
2			1	Yes	Yes
3			100	No	Yes
4	1400	10	0	No	No
5			1	No	Yes
6	1400	20	5	Inconclusive	Yes
7	1400	60	100	No	Yes
8	1500	20	0	Yes	No
9			1	Yes	No
10			100	No	Yes
11	1500	5	1	Yes	No
12	1500	10	1	Yes	No
13	1500	5	50	Inconclusive	Inconclusive
14	1500	60	100	No	Yes

Table 2.2 summarizes the results from heating a patterned SiC sample with AlN capping layer on top. Argon pressure, temperature and time were the variable process parameters. The table shows how the sample behaves – whether the SiC graphitizes, and whether the AlN sustains the high growth temperatures. For Sample # 6, the graphene-growth criterion was inconclusive. This means that some samples showed graphene,

while others did not under the same growth-conditions. As for Sample # 13, no conclusive data for either behavior was observed.

AlN degradation occurs during every growth, only the degree to which it occurs differs. When Table 2.2 lists AlN as sustaining growth, most of the AlN inhibits graphene growth. As for the opposite state, most of the AlN deteriorates, and graphene grows under it in most cases.

The surface of the samples was characterized using scanning probe microscopy and Raman spectroscopy.

Scanning Probe Microscopy:

This was performed using an atomic force microscope (AFM). Figures 2.3 – 2.6 show AFM images of various samples (Sample # indicated by the caption).

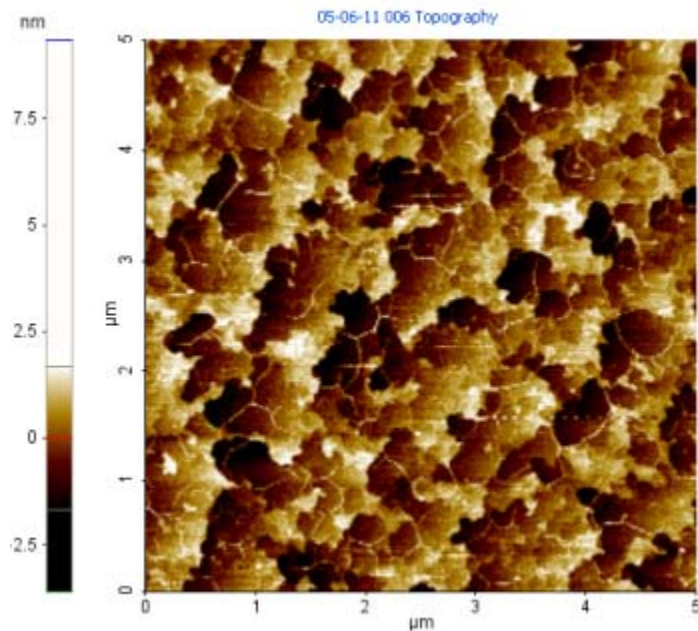


Figure 2.3: AFM of Sample # 2 (5 um scan size).

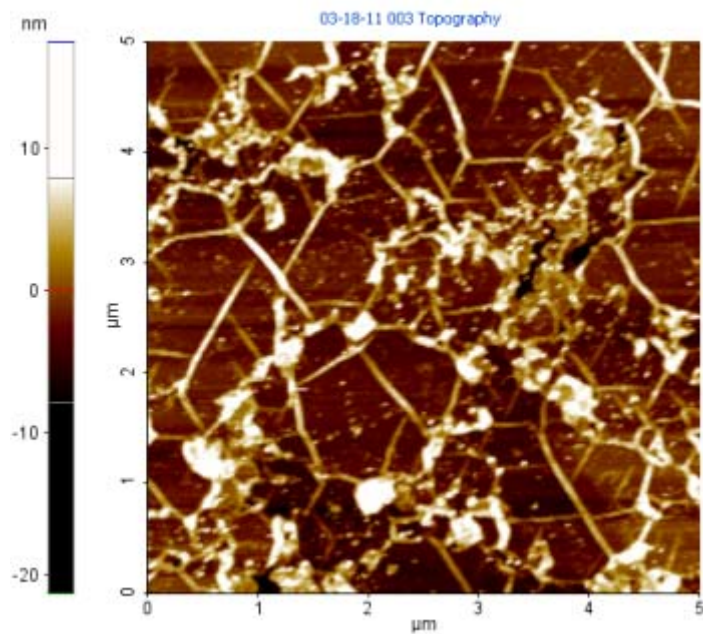


Figure 2.4: AFM of Sample # 9 (5 μm scan size).

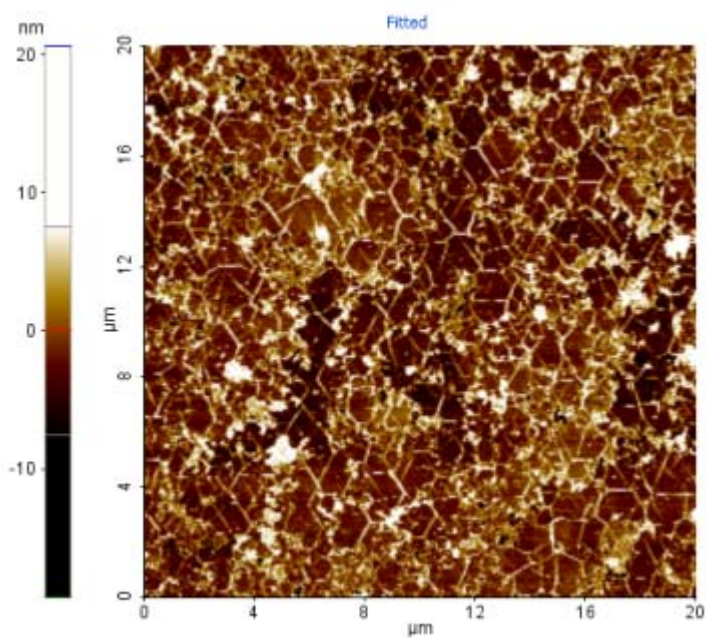


Figure 2.5: AFM of Sample # 9 (20 μm scan size).

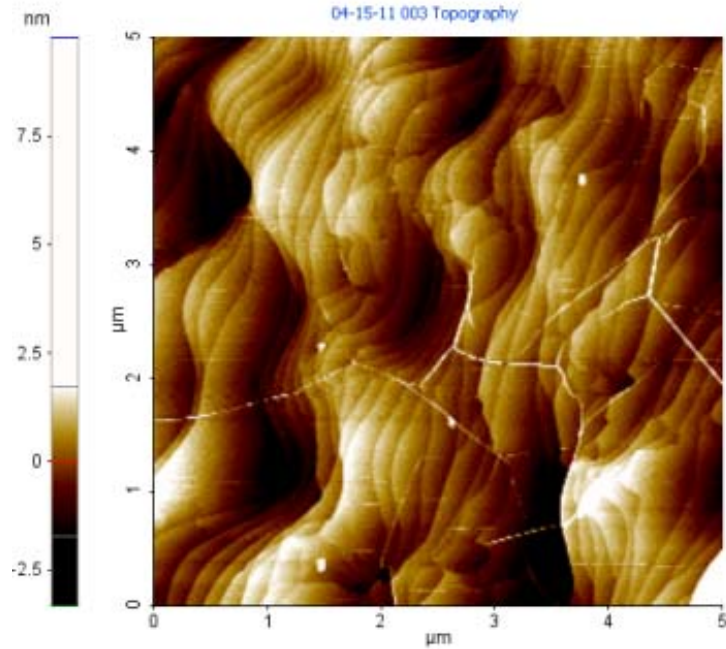


Figure 2.6: AFM of Sample # 12 (5 μm scan size).

After graphitization at various temperatures, the C-face shows pleats. The irregular black shapes in Figure 2.6 are pits in the SiC underlying the graphene film. As seen in Figure 2.6 above, graphene spreads over several SiC terraces. Boundary-scattering and substrate-induced scattering are predominantly responsible for reducing mobility in large surface area epitaxial graphene [57]. This explains the relatively modest mobility values experimentally shown by electronic transport results in Chapter 3.

Thickness of the AlN did not change significantly upon graphitization. An AlN thickness measured at 78 nm before graphitization (by AFM) reduced to 74 nm after the process.

Raman Spectroscopy:

The Raman spectral images of various samples are shown in Figures 2.7 – 2.12.

The caption of the figures shows the sample # imaged.

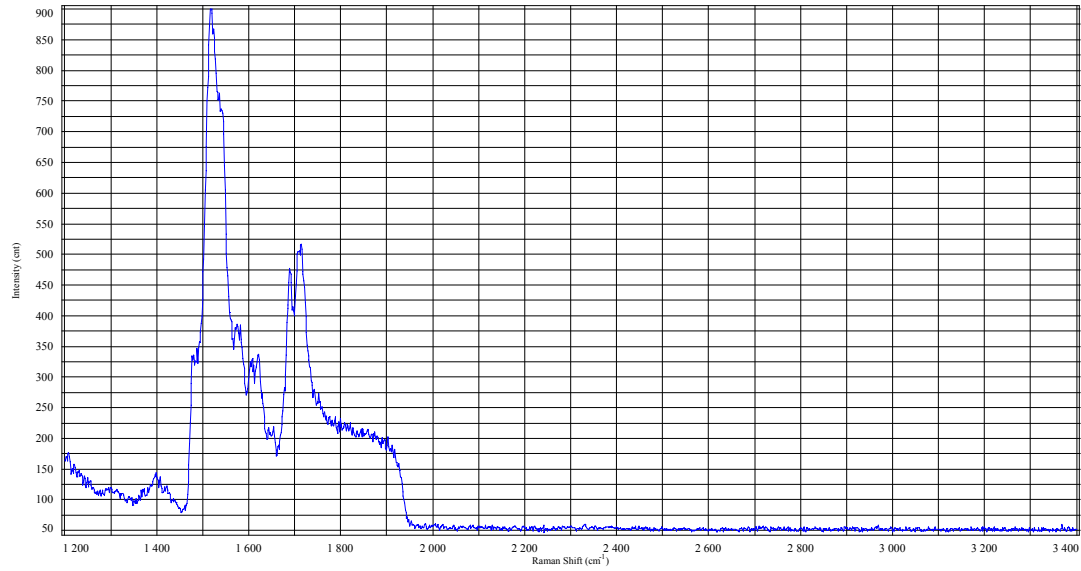


Figure 2.7: Sample# 2 Raman (AlN-capped area inhibiting graphitization).

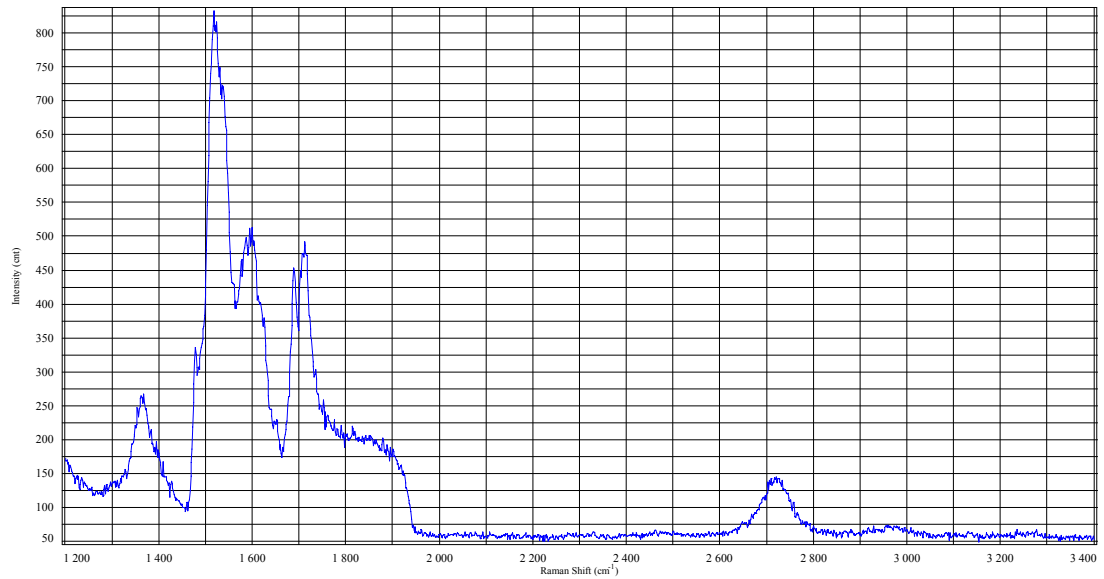


Figure 2.8: Sample# 2 Raman (AlN-capped area with graphene growing under it).

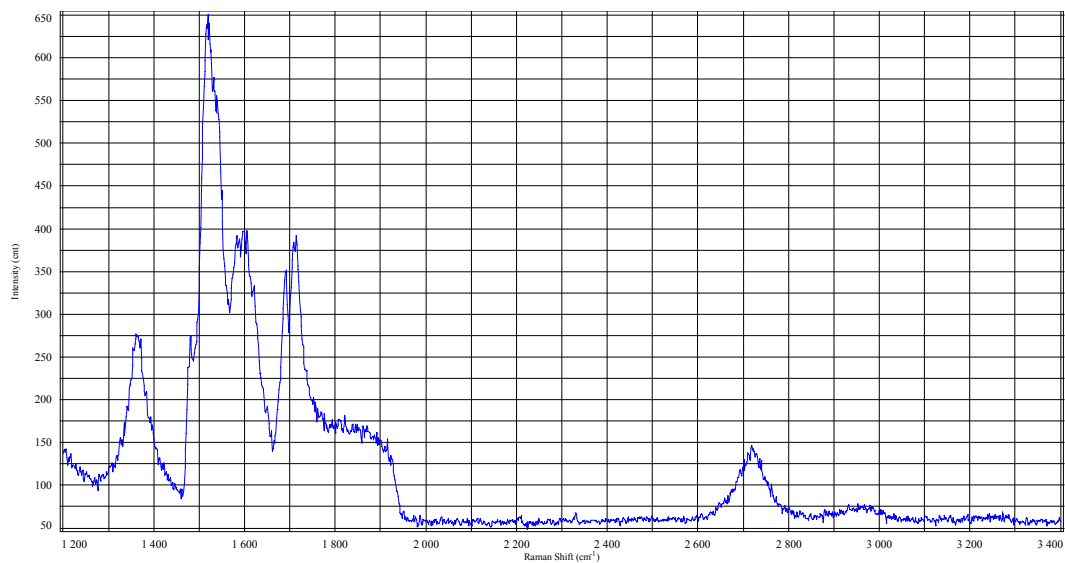


Figure 2.9: Sample# 2 Raman (Non-AIN area with graphene).

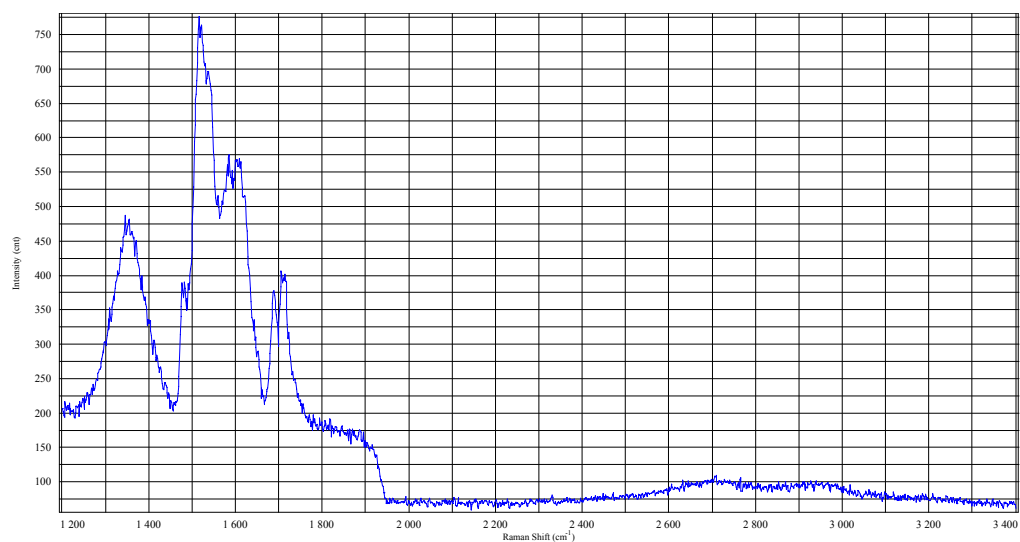


Figure 2.10: Sample# 2 Raman (Non-AIN area with disorder within graphene).

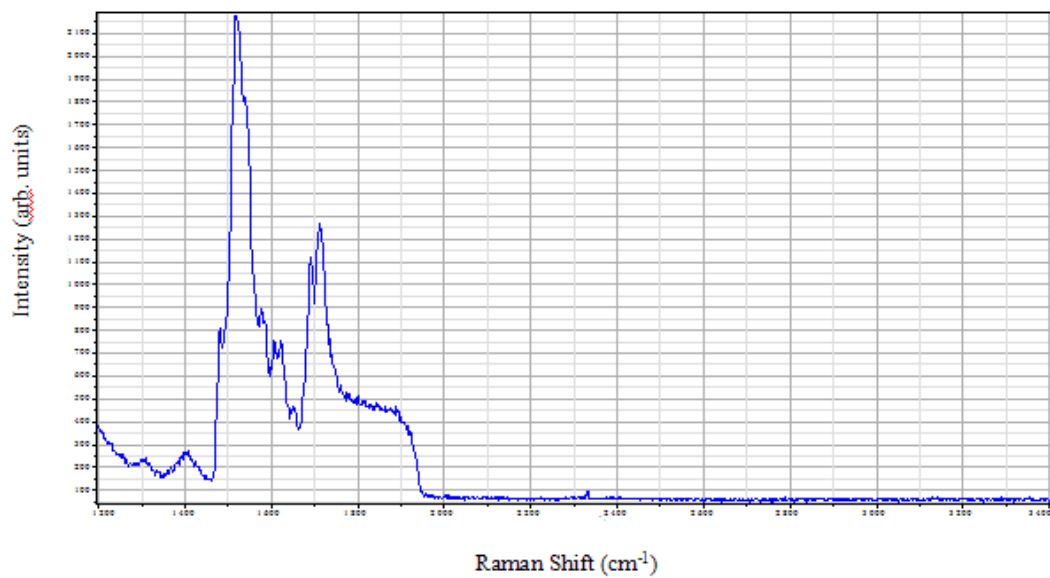


Figure 2.11: Sample# 5 Raman (also representative of bare SiC).

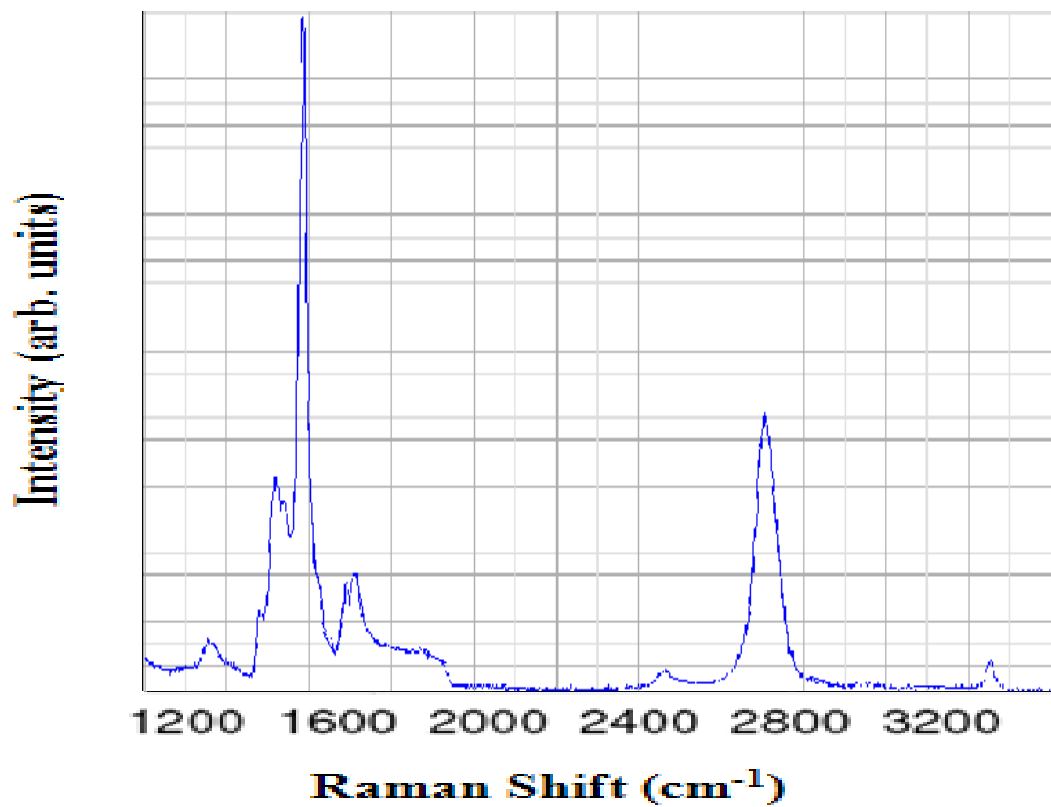


Figure 2.12: Sample# 9 Raman.

The most important features of the Raman spectra are the G band at $\sim 1584 \text{ cm}^{-1}$ (due to the E_{2g} vibrational mode) and the 2D band at $\sim 2700 \text{ cm}^{-1}$ (second-order two-phonon mode) [58]. A third feature, the D band at $\sim 1350 \text{ cm}^{-1}$ is observed as well indicating a high density of defects (as illustrated in Figure 2.4). The defects in the samples also lead to the relatively low mobility observed in the graphene Hall-bar structures, explained further in Chapter 3.

Since the ultimate motivation behind selective graphitization is to obtain high-mobility graphene for high-speed electronic applications, AlN was only deposited on the C-face. This is because graphene on the C-face has been observed to have higher mobility than that on the Si-face [45]. Therefore, selective graphitization was not demonstrated on the Si-face, however the impact of growth conditions was still investigated. Table 2.3 summarizes the different experiments performed on the Si-face by altering various process parameters in argon-environment.

Table 2.3: Table summarizing behavior of Si-face under different growth-conditions.

Si-face	Growth Conditions			Does graphene grow?
Sample #	Temperature ($^{\circ}\text{C}$)	Time (min)	Argon Pressure (mbar)	
1	1400	20	1	No
2			100	No
3	1400	60	1	No
4	1500	60	1	Inconclusive
5	1600	10	1	Inconclusive

2.5 Impact of Process Parameters on Graphene Growth

Effect of SiO₂ Etch Mask:

The goal of selective graphitization is to grow graphene in areas not covered by AlN capping layer. To accomplish this, desired regions of AlN need to be etched away. Previously, resist (PMMA for e-beam lithography or Shipley 1813 for photolithography) was being used as the etch-mask to open up the necessary areas by patterning and etching (Appendix A). Upon graphitization, it was observed that parts of the AlN capping layer also degraded and led to graphitization, as shown in Figure 2.13. The bright regions are graphitized, and graphitization is not confined to the patterned structure. Parts of the AlN are also affected. This was believed to be due to the ineffectiveness of resist as the etch mask, hence leading to some AlN etching even within the capping layer.

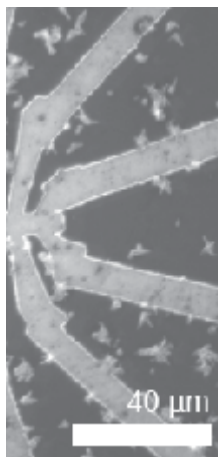


Figure 2.13: Degradation of AlN capping layer. The dark regions indicate AlN, while the bright spots within the AlN indicate graphitization.

To eliminate this problem, silicon dioxide was deposited on AlN to act as a more robust etch mask. The process is illustrated in Appendix A. However this still did not prevent graphitization within the AlN capping layer, and areas of the AlN were still undesirably graphitized. The issue is therefore believed to be a consequence of using

AlN itself, and is considered to be a fundamental limitation of the process, as detailed in Chapter 4.

Effect of Growth Conditions:

All of these results come from the C-face. The growth conditions investigated were argon background pressure, graphitization temperature, and process time.

Pressure:

Method 1: Under High Vacuum

The AlN layer did not sustain the graphitization process under high vacuum due to the higher evaporation rate of AlN. Raman signatures of the graphene were obtained from the Raman system in Dr. de Heer's research lab at Georgia Tech Physics. Micro Raman spectroscopy (Jobin-Yvon LabRAM HR800), with a 50x lens working at 532.09 nm and a diffraction network of 600 lines/mm, was used in the characterization of graphene.

A single-component (Lorentzian) 2D peak, a feature of double-resonance Raman scattering signal, is a fingerprint of simple electronic bands of graphene [59]. Graphene shows a single-component 2D band while a multi-components 2D band is observed upon increasing the number of layers in Bernal stacked graphitic structures. The 2D band appears as a single symmetrical component located at 2640 cm^{-1} (for a $\lambda=632.8\text{ nm}$ excitation wavelength) for mono-layers but shows more complex shapes as the number of layers increases.

Few layer graphene (FLG) on C-face SiC substrates is not Bernal-stacked. Instead, these layers are generally rotated at specific angles. Consequently, the sub-lattice symmetry is not lifted in the multilayers and Raman scattering spectra exhibit a single-

component 2D peak. The stacking of FLG on SiC has been determined from X-ray reflection measurements to show an interlayer distance of 3.368 ± 0.005 angstroms, that is intermediate between that of highly ordered pyrolytic graphite (HOPG) and the one found in turbostratic graphite [45].

Graphene formed using MBE AlN as a capping layer exhibits a 2D peak with minimal shoulders, as seen in Figure 2.14. The intensity of the peak also does not vary much across the $5\mu\text{m} \times 5\mu\text{m}$ mapping area. This observation could be an indication of the growth of uniform graphene.

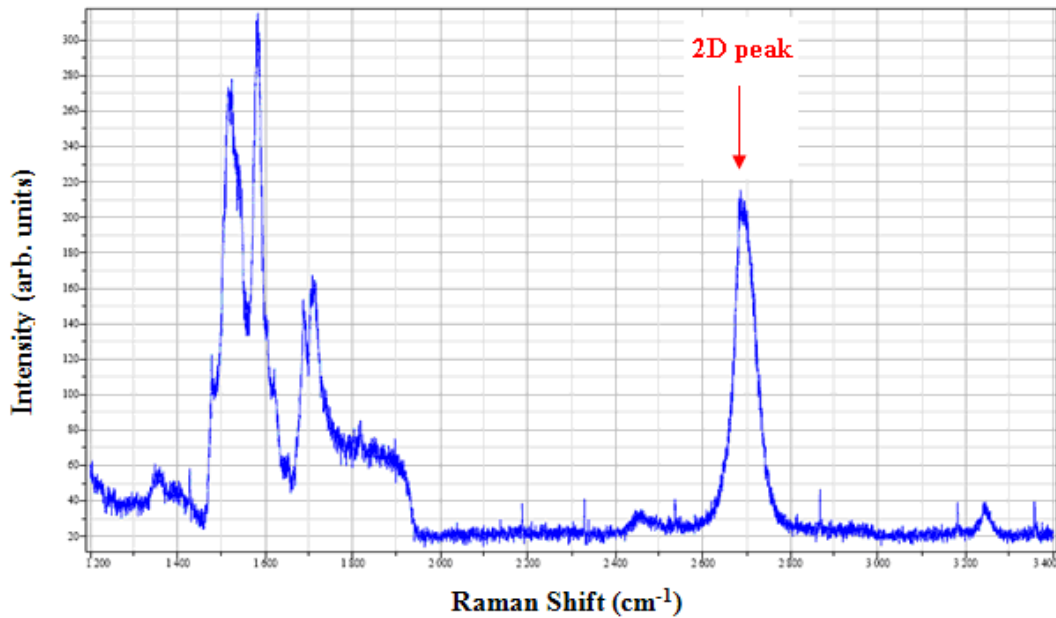


Figure 2.14: Raman signature of graphene formed under high vacuum.

Method 2: Under Ar Pressure

The argon background pressure was found to be crucial in the selective graphitization process. Argon pressure of 100 mbar inhibited growth even in non-capped regions, while high vacuum allowed growth over the entire surface, both capped and non-

capped areas. With an intermediate Ar pressure of 1 mbar for 20 min, the MBE AlN withstood high graphitization temperatures of 1400°C inhibiting graphene growth significantly. In an Ar pressure of 1 mbar, graphene was formed in regions not capped by AlN. This selective graphitization method provided an effective technique for generating electronic-quality graphene. A graphene thickness of about 0.6 nm (characteristic of bilayer graphene [45]) to 1.5 nm (FLG) was measured by an ellipsometer in Dr. de Heer's lab. Figure 2.15 shows a map of the 2D peak intensity over the patterned area of the sample graphitized at 100 Pa.

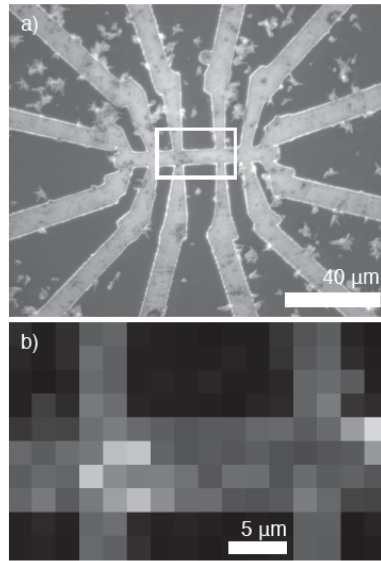


Figure 2.15: Raman spectral map of a graphene hall-bar patterned using AlN capping. a) Optical microscope image with a rectangle delimiting scanned area. b) 2D band intensity of the scanned area. The characteristic Raman signal for graphene primarily appears in non-capped areas.

Raman spectra were collected on SiC in regions both with and without the AlN capping layer following the graphitization process. The Raman spectrum of the capped SiC area (Figure 2.16-a) is exactly the same as that of bare SiC, proving the effective

capping of AlN leaving the SiC surface ungraphitized. On the other hand, there are 3 prominent peaks in the exposed SiC area (Figure 2.16-b) – G, 2D, and D peaks. The G peak ($\sim 1584.3\text{cm}^{-1}$ with FWHM 32cm^{-1}), which comes from the breathing mode for graphitic material, proves the existence of carbon material [59]. The symmetric 2D peak ($\sim 2700.6\text{cm}^{-1}$ with FWHM 58cm^{-1}), which originates from a two-phonon double resonant enhancement, clearly identifies high-quality graphene. In contrast to regular epitaxial graphene which shows no D peak, the D peak (1348.4cm^{-1} with FWHM 42cm^{-1}) in the exposed SiC area indicates a certain amount of defect in the graphene system (possibly due to islands).

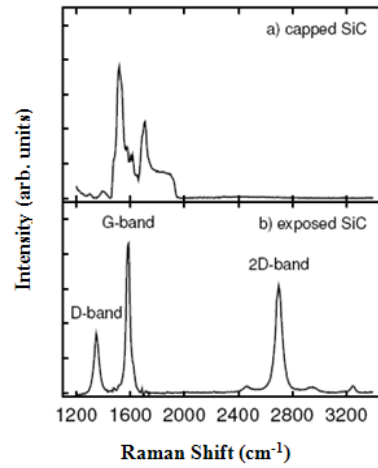


Figure 2.16: Raman spectrum of the AlN and non-AlN capped regions. a) Raw micro Raman spectrum of an AlN-capped spot (i.e. outside the patterned area). b) Spectrum of an exposed $2\mu\text{m}$ spot (i.e. patterned area), after subtraction of the SiC contribution.

The observation of a single-Lorentzian 2D peak in the Raman spectrum supports the existence of two-dimensional Dirac-like electronic states in the graphene grown using MBE AlN as capping layer, maintaining the expectations of its possible use in functional devices.

Temperature:

- At 1400°C for 20 minutes, few-layer graphene is obtained
- At 1500°C for 20 minutes, much thicker graphene seen

Time:

- At 1400°C for 10 minutes, no graphene growth occurs
- At 1400°C for 20 minutes, graphene growth is observed

Several runs of graphitization were performed on C-face with AlN on SiC. After much parameter changes, the following conditions give the most optimal results:

Sample: 4H-SiC (C-Face; Hydrogen-etched)

Temperature: 1400°C

Time: 20 min

Argon Pressure: 1 mbar introduced at 1200°C

Cool-down Rate: 50°C/min

2.6 Summary

This chapter demonstrates the use of AlN (deposited by MBE) as an encapsulant for subsequent selective graphitization. AlN with its high temperature resistance and lattice and thermal expansion matching to the SiC substrate is deemed the most suitable candidate as a capping material. MBE is a more repeatable process for AlN capping using metal modulation epitaxy process (MME), along with reflection high energy electron diffraction (RHEED) exposure. The AlN thus deposited showed <002> crystallinity, and generated uniform graphene.

Electronic-quality epitaxial graphene was selectively grown on SiC in areas not capped by the AlN. To demonstrate this, first-ever electronic transport measurements (detailed in Chapter 3) are performed on graphene grown by this pioneering technique. The thickness of the graphene is bi-layer to few-layer graphene. The argon (Ar) pressure during growth was an important parameter for the selectivity of the graphitization process. High Ar pressure of 100 mbar inhibited growth even in non-capped regions, while high vacuum allowed growth over the entire surface. With an intermediate Ar pressure of 100 Pa for 20 min, the MBE AlN withstood high graphitization temperatures of 1400°C significantly inhibiting graphene growth under it.

The method of selective epitaxial growth of graphene on SiC described in this chapter suitably eliminated any unnecessary contact with external chemicals. The AlN is patterned and etched to open windows on the SiC surface for subsequent graphitization. By performing these processing steps on the AlN, the resulting graphene is essentially untouched by any extraneous matter, producing high-quality material, as indicated by a single-component Raman 2D peak (Figure 2.14). The successful graphitization of desired regions with minimal D peak would pave the way to the development of graphene-based device architectures.

CHAPTER 3

ELECTRONIC TRANSPORT IN SELECTIVE EPITAXIAL GRAPHENE

3.1 Introduction

This chapter describes the fabrication of Hall-bar structures for electronic transport measurements. Two methods have been investigated to obtain graphene in the desired pattern – first, dry etching of AlN and e-beam lithography (Method 1), and second, wet etching of AlN and photolithography (Method 2).

Hall-bar structures were patterned on AlN using e-beam lithography (JEOL JSM-5910 system) [34], and alternatively, using photolithography. Following AlN etch and subsequent graphitization, 100 x 5 μm (Method 1) and 70 x 5 μm (Method 2) graphene Hall-bars were fabricated. Hall Effect measurements were then made on the Hall-bar structures using the probe-station (Stanford Research SR830 lock-in).

Hall measurements are widely used to measure carrier concentration and carrier mobility in semiconductors [60]. The Hall Effect (discovered in 1879 by Edwin Hall) is the production of a voltage difference (referred to as the Hall voltage) across an electrical conductor. This voltage is transverse to an electric current in the conductor, and a magnetic field perpendicular to the current, given by the equation:

$$V_H = \frac{RIB}{w}$$

where V_H is the Hall voltage, R is the Hall coefficient, I is the electric current, B is the magnetic induction, and w is the sample thickness.

In simple conductors (with only one type of majority carriers, either electrons or holes), the Hall coefficient, R is defined by

$$R = \frac{-1}{nq}, \frac{1}{pq}$$

where q is the electronic charge and n or p is the carrier density. The carrier type and the concentration can therefore be determined from the Hall coefficient. Hall mobility is subsequently determined by the equation,

$$\mu_H = \frac{R}{R_s}$$

where μ_H is the Hall mobility, R the Hall coefficient, and R_s is the sheet resistance. The sheet resistance is obtained using a four point probe (to avoid contact resistance). A constant current is applied to the two probes, and the voltage is measured on the other two probes with a high impedance voltmeter. The current and the voltage values give a measurement of the resistance using Ohm's law, Resistance = Voltage/Current. The resistance is also given by $R_s \frac{L}{W}$, where R_s is the sheet resistance, L and W the length and width of the sample. Using this equation, the value of R_s is obtained to calculate mobility.

3.2 Fabrication of Graphene Hall-Bar Structures

3.2.1 Etching AlN

AlN was deposited using MBE. Once the SiC surface was capped with AlN, the film was etched away from selected regions using both wet and dry etching methods.

Method 1: Wet Etching

Chemical: 1% TMAH (tetramethylammonium hydroxide)

Temperature: Room temperature

Time: 30 s

Method 2: Dry Etching

Machine: Plasmatherm ICP (at Georgia Tech NRC)

Gas Flow: Cl_2 (32 sccm), BCl_3 (4 sccm), and Ar (5 sccm)

Power: 500 W (Coil); 70 W (Platen)

Pressure: 5E-3 Torr

DC Bias: 250-275 V

Time: 60 s

The good crystallinity of the MBE AlN renders wet etching difficult due to its chemical inertness. Wet etching (Method 1) of the high-quality AlN film using TMAH has a low etch-rate, sometimes only being etched through inter-grain defects [61]. Figure 3.1 shows small AlN residue particles still remain after wet etching.

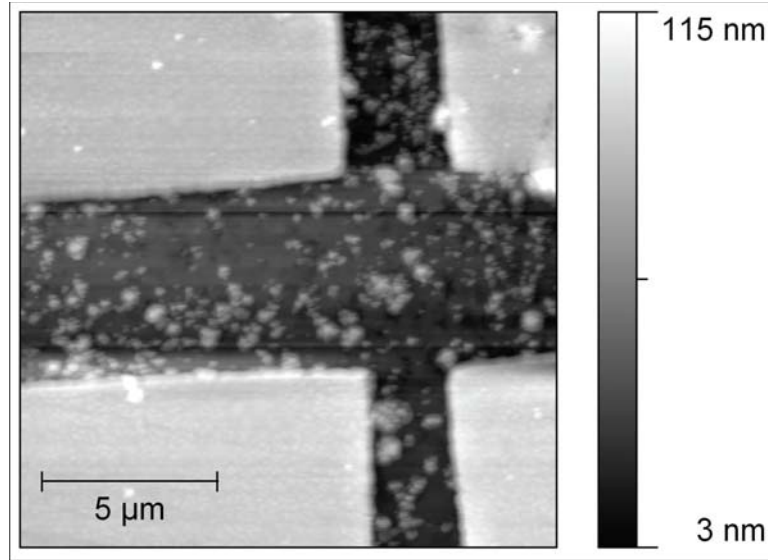


Figure 3.1: Non-contact AFM topography image of part of a hall bar graphitized under 100 Pa Ar pressure using MBE AlN as a capping layer. Small AlN residue particles are visible.

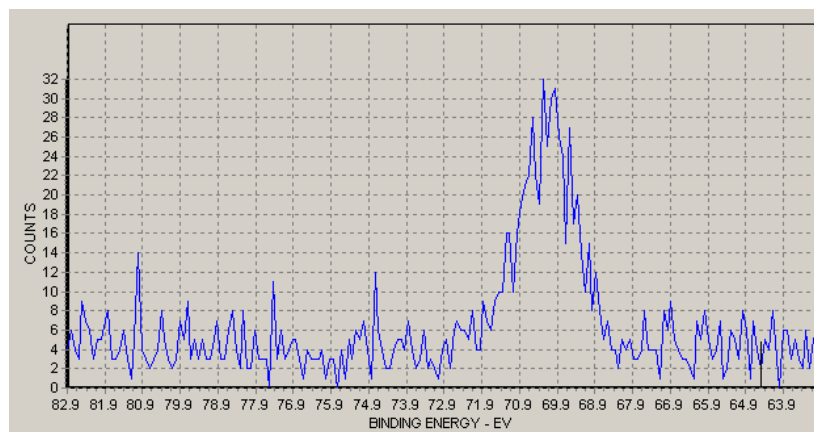
Higher Al flux can lead to defects in the AlN film. AlN is very sensitive to its Al flux. Excess Al has a tendency to solidify in the AlN creating defects within the film. Wet etching seems to attack these defects in between highly crystalline AlN columnar structures, generating a SiC surface roughness of about 10 nm (measured by the AFM). The fact that some Al may be building up in the AlN can be derived from RHEED patterns. With each subsequent MBE run, the quality of the AlN has improved with optimizing the Al flux. Therefore, dry etching needed to be performed.

The AlN thickness used in these experiments is 80 nm, which was chosen because of the balance this thickness provided between the ease of etch of AlN, and its effective capping ability. Initially, the etch mask used during AlN dry etch was the resist alone. This may have caused low-grade etching through pinholes even in the non-etched regions of the sample. In subsequent runs, a layer of silicon dioxide (SiO_2) was deposited on the AlN as the etch mask in the hopes of preventing detrimental effect to the sample.

A further area of improvement was in the gases used. BCl_3 leads to surface polymerization for anisotropic etching, which means the side-walls are polymerized during etching. This process may have resulted in the deposits found on the SiC surface after etching in initial runs. By reducing the flow rate for this gas, it was believed that the residues were eliminated leading to a higher-quality SiC surface for subsequent graphitization (Figures 3.2 – 3.4). The surface roughness measured after dry etching was 1.5 nm.

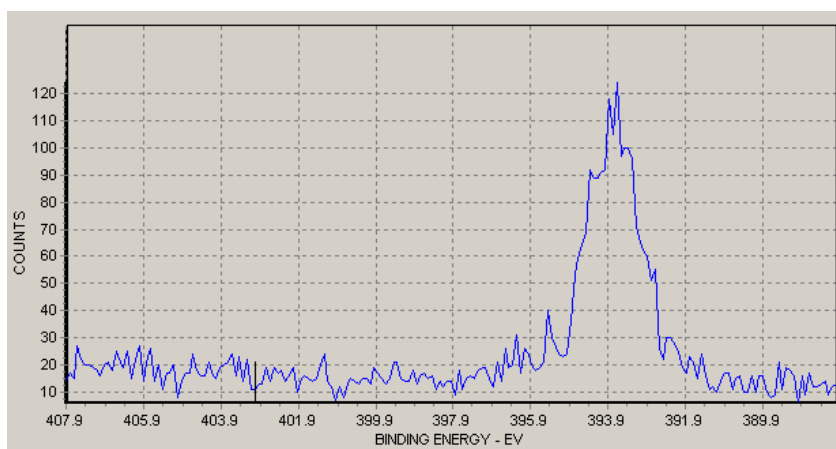
AFM imaging is performed on the etched samples to check for any residues left by the etching process and to analyze surface quality of SiC. XPS analysis further determined the quality of etch confirming that AlN is completely etched away from the desired regions (Figures 3.2-3.3). Prior to AlN etching, Hi Resolution XPS showed Al peak at 70.5 eV and N peak at 394 eV, as shown in Figure 3.2.

(a)



Al

(b)



N

Figure 3.2: XPS analysis of AlN before etch. Hi Resolution XPS of (a) Al (peak observed at 70.5 eV), and (b) N (peak observed at 394 eV).

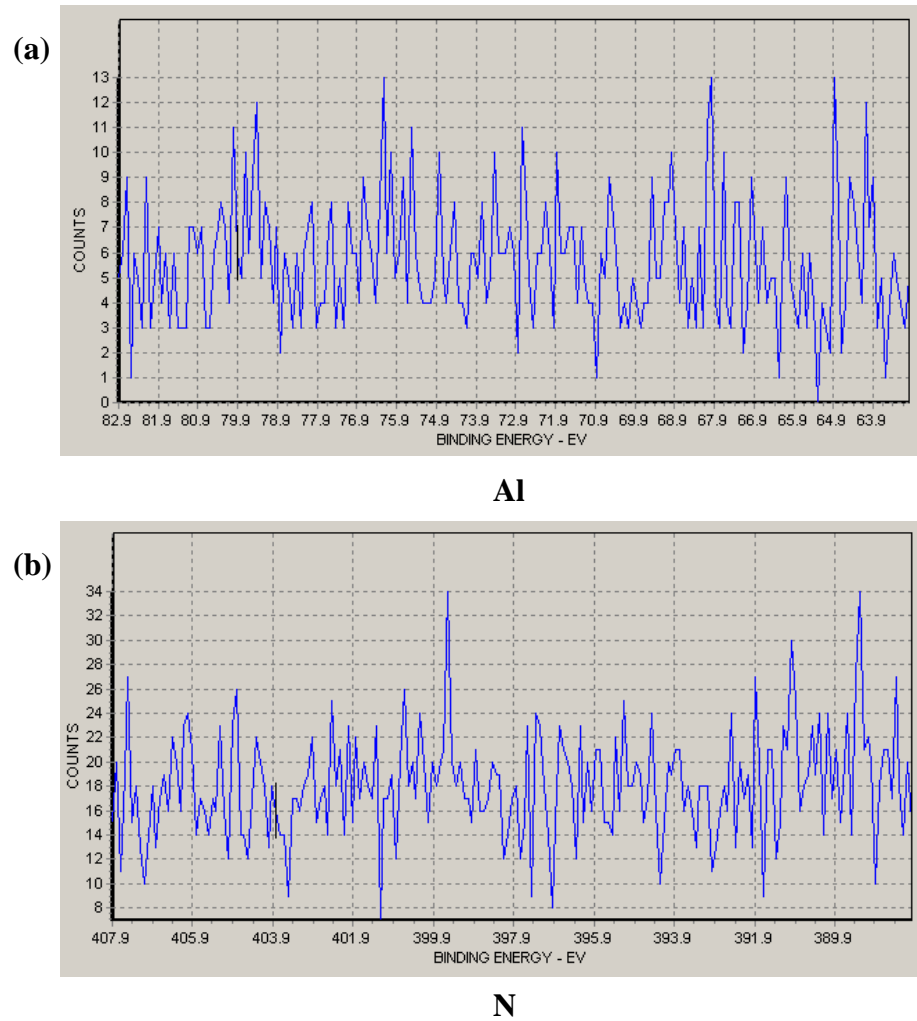
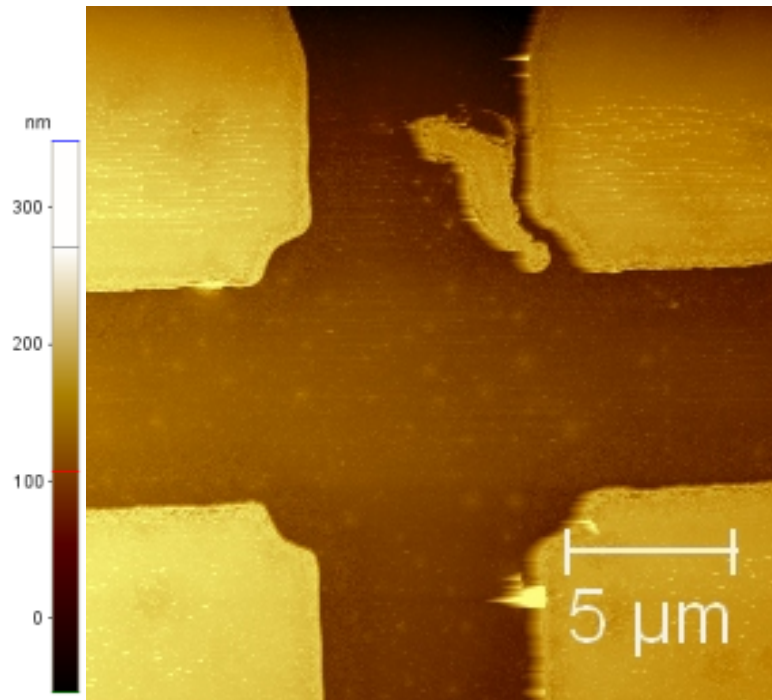


Figure 3.3: XPS analysis of AlN after etch. Hi Resolution XPS of (a) Al, and (b) N. No peaks observed for both.

Following the etch, no discernible peaks were shown, as seen in Figure 3.3.

Figure 3.4 shows the AFM image of the etched structure.



Dry Etching

Figure 3.4: AFM topography of Hall-bar structure with negligible residues.

3.2.2 Lithography

Method 1: Electron-Beam Lithography

E-beam lithography (in Dr. Walt de Heer's lab) was initially used to pattern a Hall-bar structure using 1.5 μm of PMMA e-beam resist. The channel-dimensions are 5 μm x 100 μm, as indicated by the rectangle in Figure 3.5.

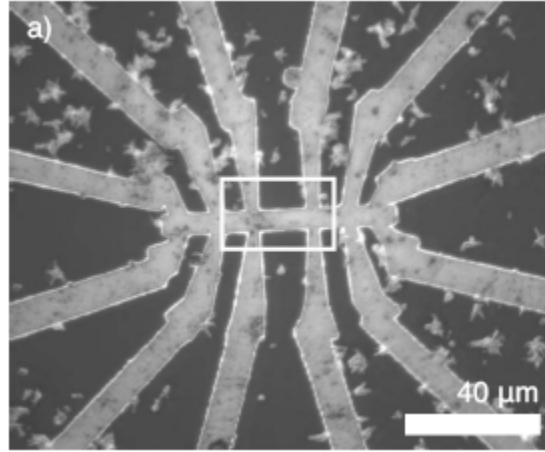


Figure 3.5: Graphene Hall-bar structure fabricated with e-beam lithography and wet etching.

Method 2: Photolithography

Subsequently, photolithography was used to fabricate graphene Hall-bar structure using 1.3 μm of Shipley 1813 positive photo-resist. The Hall-bar pattern with channel-dimensions of 5 μm x 70 μm is shown in Figure 3.6. The bright patterned area indicates graphene. The uneven edges and the isolated spots are characteristics of selective epitaxial graphene growth, and are discussed further in Section 4.2. In this chapter, electronic transport results on the graphene Hall-bar structures are presented.

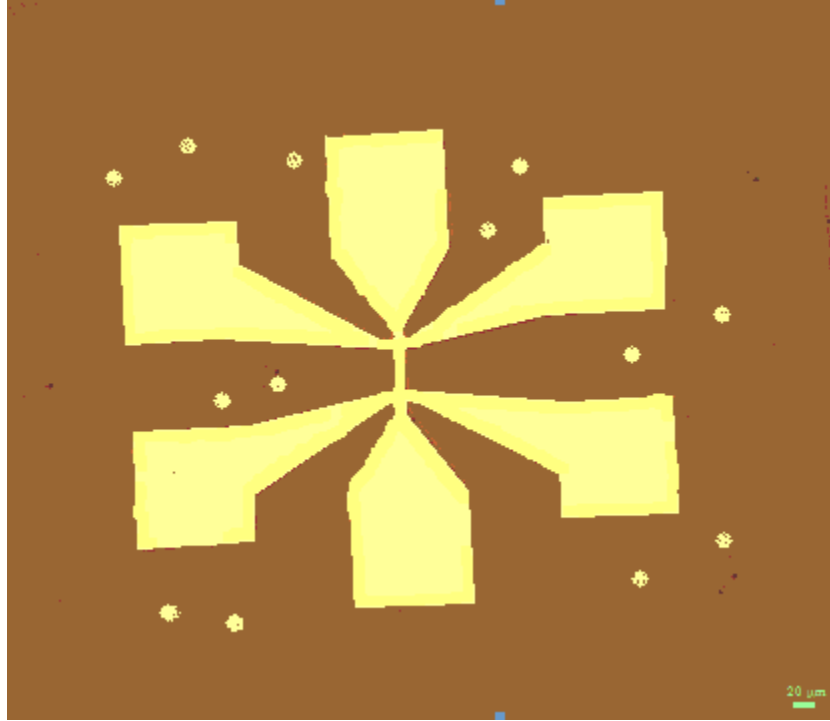


Figure 3.6: Graphene Hall-bar structure fabricated with photolithography and dry etching.

3.2.3 Yield

With e-beam lithography, the number of Hall-bars fabricated on one sample (3.5 mm x 4.5 mm) is limited to the pattern-time. In our experiments, two Hall-bars were patterned every run. Photolithography allows for a higher number of Hall-bars in relatively less time. Using an optical mask, about 6 Hall-bars were patterned onto our sample in each run. Unfortunately, not all of the structures yielded transport results (Section 3.3). This indicates the extreme sensitivity of the graphene growth.

The challenges facing this selective graphitization process are enumerated in Section 4.1, with recommendations for improvement in Section 4.3. A high-yield of graphene devices is envisaged upon optimization of this process.

3.3 Transport Studies of Selective Graphene

In the structures investigated in this chapter, electronic transport is measured by the classical Hall Effect. Hall-bar structure measurements determine

- Sheet Resistance
- Carrier Density
- Mobility

The mobility of charge in a semiconductor determines the electronic quality. This governs the speeds the material is able to provide in electronics. Two different factors slow down the movement of charge. The first factor is a “built-in” speed limit that cannot be changed: ripples in the sheets trap vibrations from heat passing through the graphene, which in turn slow down the traveling electrons. The second source of electron congestion is impurities in the graphene. These could be removed, however, via better manufacturing, meaning the material’s electronic quality should reach the proposed record-breaking levels ($10^6 \text{ cm}^2/\text{Vs}$). To our knowledge, these are the first transport measurements on selectively grown epitaxial graphene using AlN as an encapsulant [34].

Electrical transport measurements were carried out with a Stanford Research SR830 lock-in probe-station at room-temperature using an electromagnet of 0.85 T and current of 10 nA. The transport results are as follows [34]:

Method 1

- ❑ **Sheet Resistance:** $1 \text{ k}\Omega/\square$
- ❑ **Sheet Carrier Density:** $(1.08 \pm 0.06) \times 10^{13} \text{ cm}^{-2}$
- ❑ **Hall Mobility:** $580 \pm 80 \text{ cm}^2/\text{Vs}$

The value of Hall-mobility is quite high ($\sim 600 \text{ cm}^2/\text{Vs}$) considering the etch-residues (Figure 3.1) on the SiC surface, and much higher mobilities ($\sim 1550 \text{ cm}^2/\text{Vs}$) were obtained with improved etching and graphitization processes (Method 2). The sheet carrier density is rather high indicating possible doping of graphene by the residues. The elimination of the residues by improving the etch step reduced the electron density and smoothened the surface, which in turn increased electron mobility, as shown by the following results.

Method 2:

- Stanford Research SR830 lock-in probe-station
- Room temperature
- Magnetic Field: 0.15 T
- Current: 1 μA

□ **Sheet Resistance:** $0.9 \text{ k}\Omega/\square$

□ **Sheet Carrier Density:** $(4.12 \pm 0.09) \times 10^{12} \text{ cm}^{-2}$

□ **Hall Mobility:** $1502 \pm 63 \text{ cm}^2/\text{Vs}$

This modest value is attributed to the defects originating during growth due to islanding occurring at low temperatures in low-pressure argon environment [51]. The graphene shows electron-doping (n-doped). Figure 3.7 plots Hall mobility values versus sheet carrier densities obtained from electronic transport measurements on the Hall-bar structures.

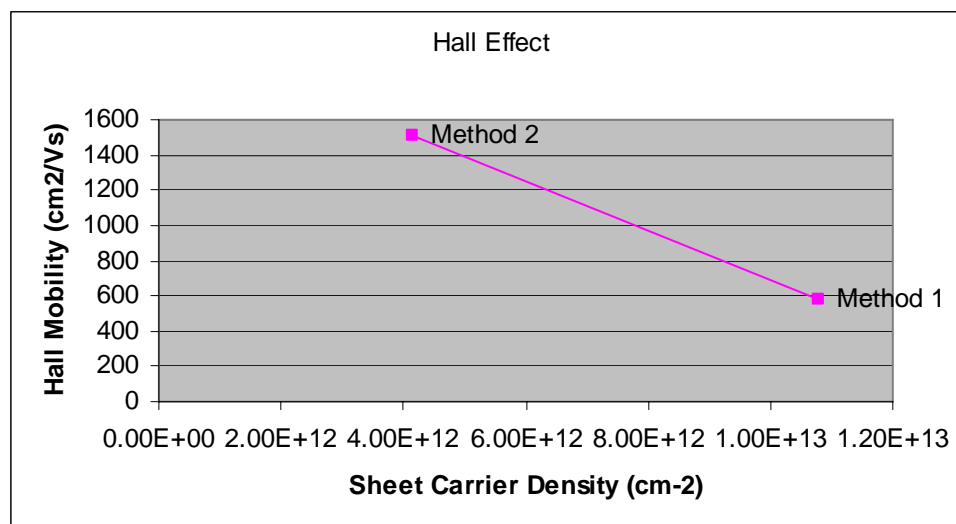


Figure 3.7: Average Hall mobility versus sheet carrier density values for selective epitaxial graphene Hall-bar structures. Method 2 shows much improved mobility results.

3.4 Summary

Graphene Hall-bars were successfully fabricated using this method with no exposure of the graphene to external chemicals, such as resists and etchants that deteriorate the performance of graphene. The highest Hall mobility measured is about $1550 \text{ cm}^2/\text{Vs}$.

CHAPTER 4

LIMITATIONS OF SELECTIVE EPITAXIAL GRAPHENE

4.1 Critical Limitations of Selective Epitaxial Graphene Growth

- Low growth temperature to prevent AlN decomposition leads to poorer quality of graphene using this process. Higher growth temperature enhances surface diffusion, ultimately leading to markedly improved surface morphology [46]. Selective growth experiments have shown that AlN does not sustain graphitization temperatures of 1500°C (Table 2.2). The upper limit of temperature is confined to 1400°C for the selective growth of graphene.
- Although AlN does not exhibit major decomposition at 1400°C, graphene still grows under certain regions of the AlN surface (Figure 4.2). This is potentially caused by the ease of sublimation of Si from these particularly vulnerable points.
- Argon-environment growth to prevent AlN decomposition leads to islanding at low temperatures on C-face. This phenomenon is also observed in [51].
- Low Hall mobility has been measured in selective epitaxial graphene thus far, possibly due to boundary-scattering. It is expected to further exasperate in smaller dimensions, therefore the D peak (Raman) needs to be minimized before investigating reduced channel-lengths.

4.2 Characteristics of Selective Epitaxial Graphene Growth

The selective graphene exhibits an edge preference during growth. According to the Raman showing 2D peak intensity (Figure 4.1), the strength of the customary 2D peak for graphene is highest along the edges of the graphene Hall-bar structure.

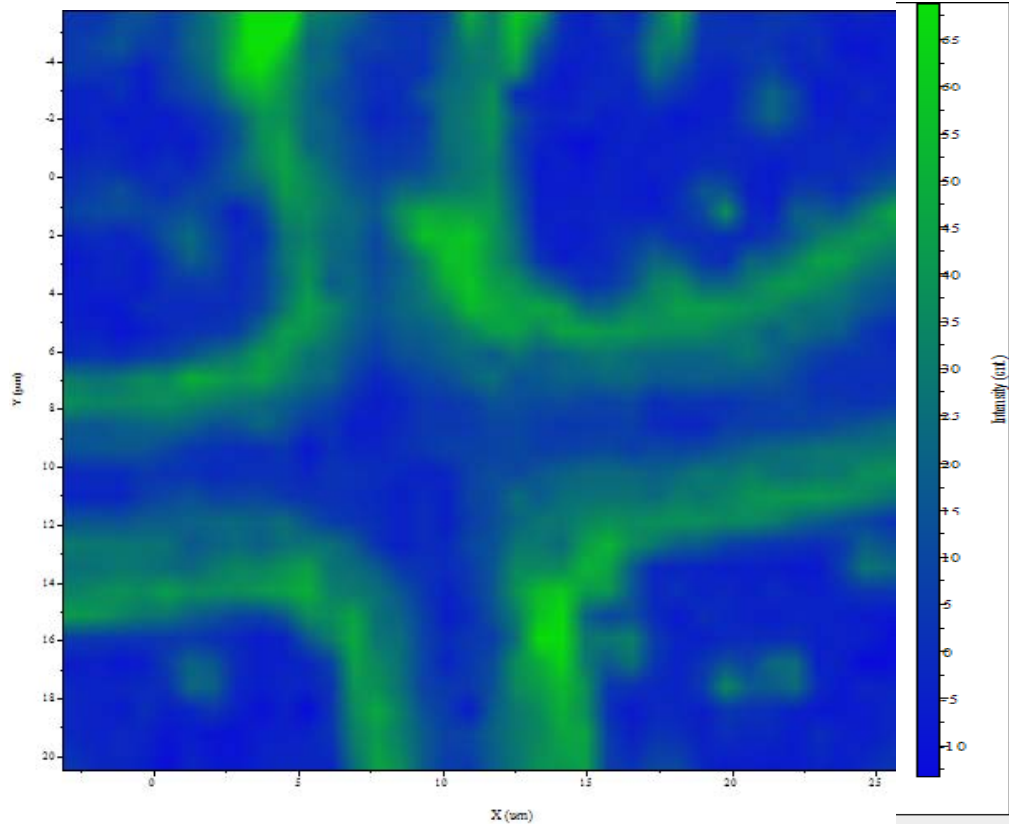


Figure 4.1: Raman 2D peak intensity appears strongest along the edges.

AFM image (Figures 2.3) of the graphene shows its pitted nature, with discernible pleats. Graphene also grew in regions within the AlN capping layer, as shown in Figure 4.2. Bright regions indicate 2D peak in Raman, and are a few nm higher than the capping layer. This increase in thickness indicates that graphene is growing under the AlN.

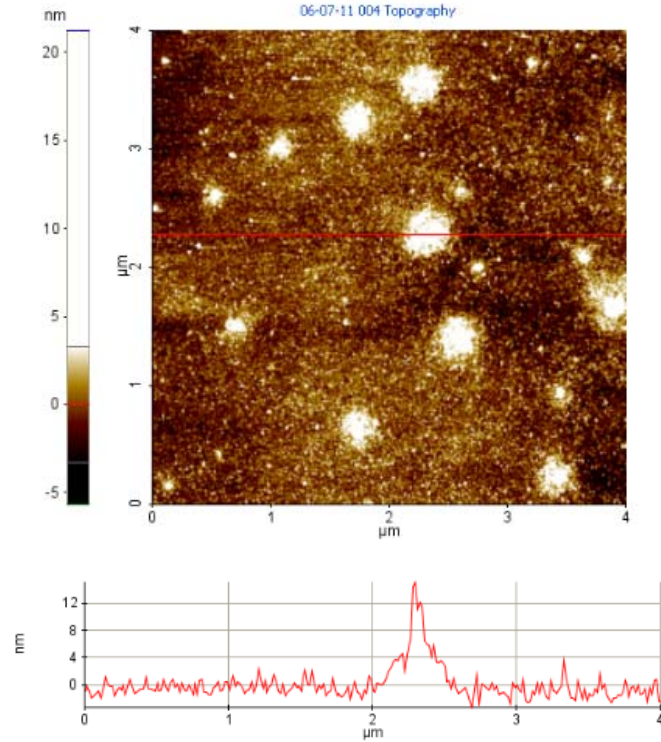


Figure 4.2: AFM of AlN capped area. Line profile (in red) indicates a rise in thickness over the bright spot. AlN covers the whole area.

Figure 4.3 shows an optical microscopy image of part of the graphene Hall-bar structure. Bright regions indicate graphene. As expected, the region uncapped by AlN (the patterned area) is graphitized. Graphene is also seen within the AlN capping layer in the form of bright spots. This indicates isolated graphene growth under AlN capping layer. Fine tuning the Ar pressure could therefore possibly provide a way to encapsulate graphene under a dielectric without intermediate atmospheric contact.

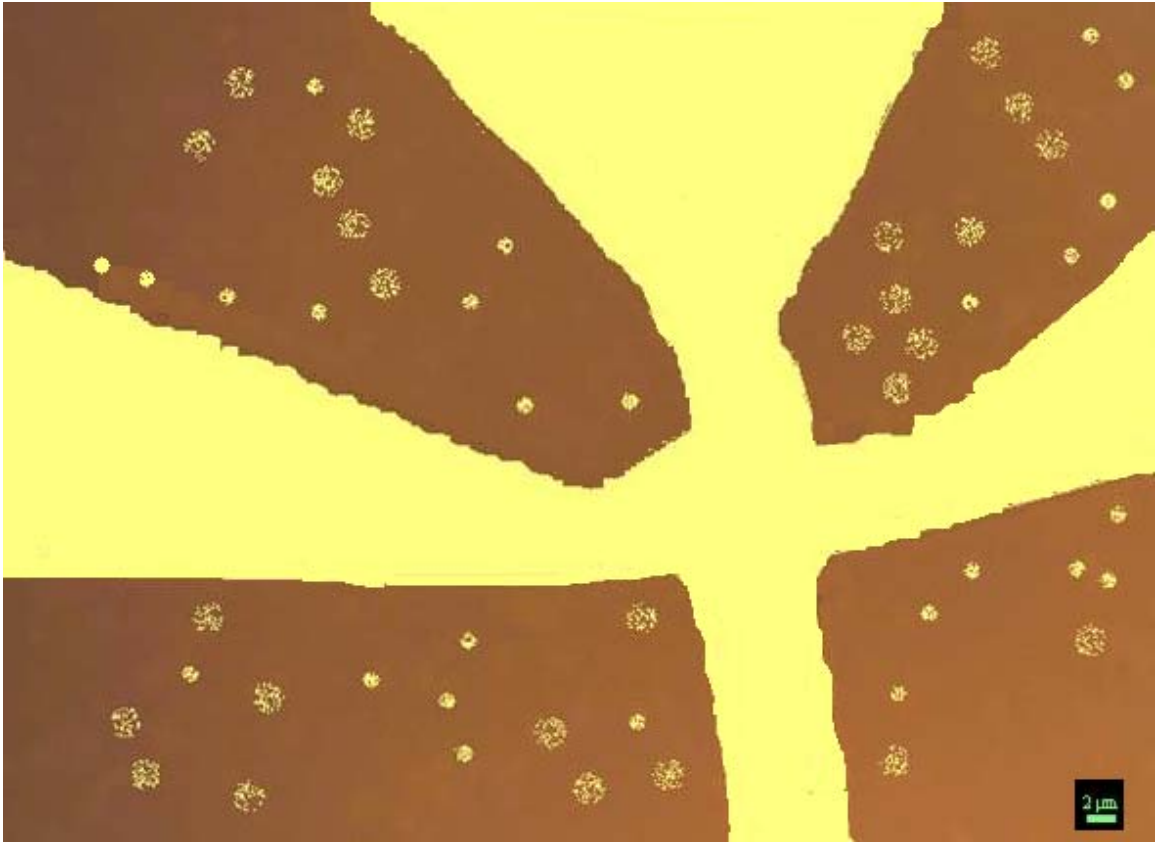


Figure 4.3: Optical image of patterned structure showing graphene growth (bright regions) within AlN capping layer.

4.3 Recommendations for Improvement

- Capping layer of AlN with BN on top to prevent AlN decomposition:*** A layer of boron nitride (by pulsed laser deposition) on top of aluminum nitride acts as a more effective capping layer. BN is more stable at higher temperatures, hence it prevents AlN from decomposing at dislocations [62]. In [62], a dual BN/AlN (300 nm/200 nm) capping layer is used to anneal implanted SiC to a temperature of at least 1700°C. Since Georgia Tech does not possess the capability to deposit BN at this time, this idea was not implemented.

- ***With a better capping layer in place, higher Ar pressure and higher temperature can be used, leading to fewer defects:*** Lower temperature graphene-growth in an argon-environment can lead to pit-formation [51]. Higher Ar pressure leads to greater domain-size and demonstrated higher mobility on the C-face.
- ***More precise control of background pressure:*** Graphitization of SiC occurs by confinement controlled sublimation (Dr. de Heer group) whereby the sublimation of silicon is controlled at the right temperature inside a confined chamber. Precise control of the rate at which silicon comes off the wafer is essential since it controls the rate at which graphene is produced, leading to the formation of uniform high-quality layers. The technique relies on controlling the vapor pressure of gas-phase silicon in the high-temperature furnace used for growing the graphene. Since the background pressure is critical in the formation of electronic quality graphene [51], a precise control of the pressure could lead to the fabrication of defect-free homogeneous layers of graphene.

4.4 Summary

Detailed understanding of the selective graphitization growth-process has been reached through surface-characterization of the graphene, namely via Raman spectroscopy and AFM as illustrated by Figure 4.1 and Figure 2.3 respectively. Preferential growth along the AlN boundary (Figure 4.1), and graphene with numerous boundaries (Figure 2.3) are the primary characteristics. Critical limitations (listed in Section 4.1) exist which will need to be eliminated for the implementation into devices.

CHAPTER 5

OPPORTUNITIES FOR SELECTIVE EPITAXIAL GRAPHENE

APPLICATIONS

5.1 Introduction

This chapter discusses future prospects and research opportunities for selective epitaxial graphene. Unlike previous chapters, neither fabrication nor measured results are presented. Graphene shows great potential for devices operating at high-frequency. The following sections elaborate the current state-of-the-art implementation of graphene radio-frequency field effect transistors (RF FETs), and also shed light on how mobility affects device performance.

5.2 High-Speed Radio-Frequency Field Effect Transistor

5.2.1 Principles of RF FET and Practical Applications

The 2D nature of graphene has a distinct advantage in that the drive current of the RF FET, in principle, can be scaled up by increasing the device channel width [33]. The width scaling capability of graphene is paramount to realizing high-frequency devices. RF FETs are manufactured using processes similar to those used to make low frequency transistors, regardless of whether they are low power or high power. The differences in RF FETs exist in that they are made with material with more precisely controlled material properties. More importantly, they are designed with narrow horizontal structures to permit them to function at RF [63]. The horizontal channel RF FET consists of a set of small signal FETs connected in parallel on a single chip. The lateral FET features

extremely low feedback capacitance, which results in increased stability and higher gain at high frequencies. Both of these MOSFETs are n-channel enhancement mode devices, meaning their gates require positive voltages with respect to the sources in order for the drain-source channel to conduct [63].

The current gain cutoff frequency (f_T) is an important performance parameter for an RF FET. This transistor parameter denotes the frequency at which the magnitude of the current gain reduces to unity (with the ac output short-circuited) and signifies the highest frequency at which signals are propagated [7]. The intrinsic current gain of an RF FET decreases with increasing frequency. This is the ideal $1/f$ dependence expected for conventional FETs. The maximum f_T is found to be inversely proportional to the square of the gate length (L_G), that is $f_T \sim 1/L_G^2$. This dependence of maximum f_T can be qualitatively understood based on the transient time of carriers in the transistor channel, as follows. The transistor f_T is mainly determined by the minimum time τ required for a carrier to travel across the channel, i.e., $f_T \propto 1/\tau = v_d/L_G$, where v_d is the carrier drift velocity. In the linear regime, the drift velocity is proportional to the drive field given by $v_d = \mu E_d$, where E_d is the electric field in the channel that is inversely proportional to the gate length for a given drain bias and μ is the mobility. Therefore, it follows that $f_T \sim \mu(V_D/L_G)/L_G \sim 1/L_G^2$ [33].

Short channels make for significantly higher frequency devices and higher channel current. In the current saturation region, drain current increases as drain voltage increases due to channel-length modulation effectively shortening the channel. With expected large ON-state current density and transconductance per unit of gate capacitance as compared to Si, graphene has the capability for extraordinary switching

characteristics and short-circuit current-gain cutoff frequency [27]. The limited $I_{\text{on}}/I_{\text{off}}$ ratio of graphene FETs may inhibit their application in computer logic, but RF applications hold promise. Graphene offers the possibility to extend the RF operational range into the terahertz frequencies [23]. To provide the desired gain at the frequency of operation, an RF FET with sufficient current rating and a high enough cutoff frequency (f_T) needs to be selected. A graphene RF FET possesses both current gain and power gain, even without current saturation [35]. This attribute of the graphene FET is elaborated in Section 5.2.2 with actual demonstrations of this behavior.

5.2.2 State-of-the-art Graphene RF FET Implementations

Graphene shows great potential for devices operating at high-frequency [35]. Graphene devices have been shown to exhibit current gain in the microwave frequency range (1-300 GHz) [33] using exfoliated graphene RF FETs. Cutoff frequency, f_T , as high as 26 GHz is measured with a gate length of 150 nm. An epitaxial graphene RF FET is implemented in [27]. This demonstrates that f_T was found to increase by decreasing the source-drain spacing. The low-field FET mobility is estimated to be $\sim 200 \text{ cm}^2/\text{Vs}$, which is lower than the Hall mobility of $1000 \text{ cm}^2/\text{Vs}$. So far, the highest f_T extrapolated in a graphene RF FET has been 100 GHz [35] with an electron carrier density of $\sim 3 \times 10^{12} \text{ cm}^{-2}$ and a Hall mobility between 1000 to $1500 \text{ cm}^2/\text{Vs}$. The gate length used was 240 nm, and the 100 GHz cutoff frequency exceeds that of Si MOSFETs with the same gate length ($\sim 40 \text{ GHz}$ at 240 nm). In addition to current gain, the graphene FET also possesses power gain, without reaching the saturation mode. For the 240-nm gate length, power gain was achieved up to f_{MAX} of 10 GHz. While f_T reflects the intrinsic behavior of

a transistor channel, f_{MAX} strongly depends on other factors such as the device layout and can be further enhanced, for instance, by optimizing the gate contact leads [35].

In the epitaxial graphene RF FET demonstrated in [27], the low-field FET mobility reduced to $\sim 200 \text{ cm}^2/\text{Vs}$ from the original carrier mobility of $1000 \text{ cm}^2/\text{Vs}$, leading to a cutoff frequency of 4.4 GHz. This reduction is also seen in [33] where the mobility reduced to $400 \text{ cm}^2/\text{Vs}$ after deposition of the top gate dielectric, generating a cutoff frequency of 26 GHz. In [64], a BN/graphene/BN FET is fabricated whereby the graphene is sandwiched between a substrate and a gate dielectric (both BN). This device structure can preserve the high mobility and high carrier velocity of graphene, hence enabling the next generation of high-frequency graphene RF electronics. Carrier injection velocities are estimated to be about $3.5 \times 10^7 \text{ cm/s}$ in this hybrid structure.

5.3 How Mobility Affects FET Performance

Higher mobility of electrons as majority carriers translates to higher f_T and improved high frequency power gain. As stated in the previous section (Section 5.1.1), the transistor cutoff frequency (f_T) follows the relation $f_T = v_d/L_G$, where v_d is the carrier drift velocity and L_G is the gate-length. The drift velocity (v_d) is also related to the channel-mobility (μ) and the longitudinal electric field (ϵ_L) by the equation, $v_d = \mu \epsilon_L$ [7]. From the aforementioned equations, it is inferred that mobility, μ is directly proportional to f_T , further emphasizing the fact that higher mobility is necessary for improved RF FET performance [7]. The cutoff frequency f_T is given by the relation, $f_T = g_m/(2\pi C_G)$, where g_m is the dc transconductance, and C_G is the gate capacitance [33]. This implies that f_T is proportional to g_m . The transconductance of the MOSFET decides its gain and is

proportional to hole or electron mobility (depending on device type), at least for low drain voltages. As MOSFET size is reduced, the fields in the channel increase and the dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths are reduced without proportional reduction in drain voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance.

As the channel length becomes very short, the equations for the different conventional modes of transistor operation become quite inaccurate. New physical effects arise. For example, carrier transport in the active mode may become limited by velocity saturation. As stated before, the relationship between drift velocity (v_d) and mobility (μ) in a channel is given by $v_d = \mu \epsilon_L$, where ϵ_L is the longitudinal electric field [7]. With increasing field, ϵ_L , along the channel, μ decreases. This is caused by the reduction in the mean free time between collisions due to optical phonon scattering. The saturation velocity, v_{sat} , depends on the low-field mobility, which is dependent on temperature, transverse electric field, and substrate doping concentration. When velocity saturation dominates, the saturation drain current is more nearly linear than quadratic in V_{GS} . At even shorter lengths, carriers transport with near zero scattering, known as quasi-ballistic transport. In addition, the output current is affected by drain-induced barrier lowering of the threshold voltage. The saturation velocity of graphene is estimated to be about $5.5E7$ cm/s, which is 5 times greater than that of silicon [65]. Current saturation is not observed in graphene devices. This is attributed to the fact that graphene is a zero-gap semiconductor. It is believed that velocity saturation at higher biases may lead to current

saturation. Higher mobility may be required to achieve this saturation velocity with the drain bias of practical interest.

Graphene has shown to have the highest carrier (electron and hole) mobility ($10^5 \text{ cm}^2/\text{Vs}$) at room temperature [27]. This is about 100 times greater than that of silicon. Hall mobility of graphene channels is measured to be higher than FET mobilities. Upon gating the FET, trapped charge or interface charge in the gate-dielectric layer can lead to a reduction in the transconductance and the mobility. Higher mobility enables high-frequency FET operation, since field-effect mobility, μ_{FE} is given by the equation: $\mu_{\text{FE}} = (L_{\text{ch}} g_m)/(W_{\text{ch}} C_G V_{\text{DS}})$ [66].

5.4 Challenges

Deposition of high-k dielectric for FET applications is particularly challenging. As transistors have decreased in size, the thickness of the gate dielectric has steadily decreased to increase the gate capacitance, $C = (k\epsilon_0 A)/t$, where k is the relative dielectric constant of the dielectric, ϵ_0 is the permittivity of free space, A is the capacitor area, and t is the thickness of the dielectric [7]. Higher gate capacitance leads to greater drive current and device performance. As the thickness continues to scale down, leakage currents due to tunneling increase drastically, leading to higher static power consumption and reduced device reliability. This phenomenon heralds the need for a high- κ dielectric that allows increased gate capacitance without increasing gate tunneling current.

Inherent critical limitations of the selective graphitization process (detailed in Section 4.1) have restricted the implementation of a graphene RF FET using this technique. The mobility of graphene channels is found to decrease upon gating the FET

[27, 33]. RF performance is primarily limited by this mobility degradation of graphene after oxide deposition due to trapped charge or interface charge in the gate-dielectric layer. To preserve the Hall mobility, [35] uses an interfacial polymer layer made of a derivative of poly-hydroxystyrene spin-coated on the graphene before atomic layer deposition of a 10 nm thick HfO₂ dielectric. To make a high-frequency RF FET, both a high-mobility channel and a high-k dielectric are crucial. The body of research presented in this dissertation has made significant progress in an innovative method for obtaining high-mobility electronic-grade graphene.

5.5 Summary

This chapter put forth the potential of using selective epitaxial graphene as the building block for making practical devices. The principal application presented in this chapter is a high-frequency RF FET. The impact of mobility on the performance of the transistor is described in the chapter.

CHAPTER 6

NANO-GAP FABRICATION

6.1 Introduction

A myriad of methods has been reported for the fabrication of a nanometer-scale gap between two metallic structures. These various methods include electromigration [67], e-beam lithography [68], and e-beam deposition [69], among others. The successful fabrication of such nano-scale gaps between electrodes opens the door to a variety of applications, such as, single-molecule detection, molecular electronics, and DNA detection [70]. This makes the study of nano-gaps between metallic particle-pairs important.

Metallic nano-particle pairs in close proximity to one another display surface-enhanced Raman scattering (SERS). Single-molecule detection has been predicted to be possible thanks to SERS. The SERS enhancement can be maximized by simultaneously increasing the curvature of the particles and bringing them into close proximity to one another [71, 72]. It has been shown that electric-fields at locations associated with high curvature features (spheroid tips) are higher than the spherical particle case [71]. Ordered arrays of metallic nanospheres with sub-10 nm interparticle gaps have been shown to provide SERS enhancements [72].

The interaction of light and designed metallic nano-particle structures has led to the discovery of induced localized electric-fields at the particle's surface. These intense localized fields are caused by a natural resonance that noble metal particles have with incoming light when the particles are smaller than the wavelength of light being used

[70]. This resonance is specific to the particle shape, size, material, and surrounding environment, and is generally termed the localized surface plasmon resonance (LSPR). When this resonance is induced and the resulting fields occur in the presence of biological or chemical species, spectroscopic signals from these species can be strongly enhanced. A biological or chemical molecule can lead to Raman scattering whereby the adsorbed molecule scatters a photon of light after absorbing just enough energy from the photon to excite a molecular bond. Consequently, the scattered photon has a lower energy ($E_{\text{initial}} - E_{\text{molecular bond}}$) providing a unique signature of the adsorbed molecule.

The localized field can be maximized by simultaneously increasing the curvature of the particles and bringing two particles into close proximity to one another (separations equal to or less than the particle size). The field intensity has been predicted to increase exponentially as the gap size decreases [71], and hence the presence of small gaps (5-10 nm) is crucial to achieving single-molecule detection. If SERS occurs in the presence of an enhanced electric-field, the scattered photon is intensified, leading to an enhanced Raman signal. Identification of hazardous substances, such as cyanide and anthrax, is then possible on an extremely small concentration level, bordering on single-molecule detection.

To-date, there has been no study in the literature about achieving both a small gap as well as a well-defined structure with sharp curvature. In [71], 7-8 nm gaps are fabricated but with circular particles. Bow-tie particles are fabricated in [73] but with poor feature definition. Sub-5 nm gaps are fabricated in [74] but the fabricated particles are either circular or shapeless. The work presented in this chapter focuses on the fabrication of bow-tie nano-gap structures (Figure 6.1) that are suitable for single-

molecule detection. To maximize the SERS effect, 100-nm triangular particles with sub-20 nm gaps between them have been fabricated. Of the several methods that exist for nano-gap fabrication, e-beam lithography is the most reproducible process, and this is the method that was used.

6.2 Fabrication of Nano-Gap Structures

For the fabrication of nano-gaps for this project, the state-of-the-art JEOL JBX-9300FS 100kV e-beam lithography system at the Georgia Institute of Technology Nanotechnology Research Center (Georgia Tech NRC) was used. To achieve reproducible nanometer-scale gaps, several methods have been undertaken to help increase the resolution of electron-beam lithography systems, including the use of thin resist thicknesses, beam interference, limiting apertures and thin membranes. Uniform sub-20 nm gaps essential for single-molecule detection were demonstrated. An electrode gap as small as 2.20 nm was obtained. The bow-tie nano-gap structures thus fabricated are illustrated in Figure 6.1.

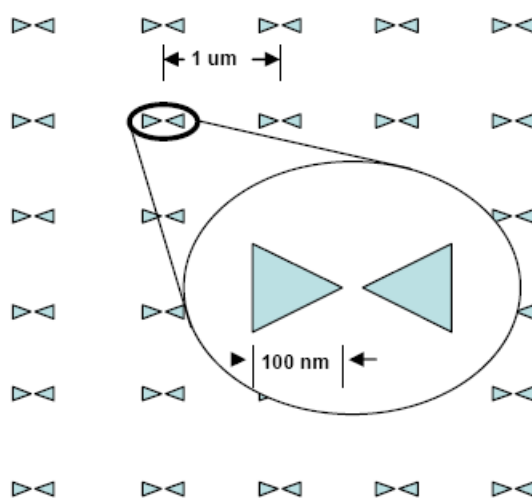


Figure 6.1: Pattern layout of metallic particle-pairs with nano-gaps.

6.2.1 Method 1: Silicon Substrate [75]

Double-side polished <100> Si wafers were used. Silicon nitride, Si_3N_4 , was deposited on both sides of the wafer using a plasma enhanced chemical vapor deposition system (PECVD) at the Georgia Tech NRC. The Si_3N_4 served a dual purpose (Figure 6.2). On the front side of the wafer, the nitride would become the substrate-membrane after through-wafer etching. On the back side, the Si_3N_4 worked as an etch mask. The front layer of nitride was very thin; experimentation was performed with thicknesses from 100-500 nm. The back layer was coated with approximately 1 μm of nitride.

After Si_3N_4 deposition, standard photolithography was performed on the back of the wafer to open up windows for subsequent nitride etch. Using an inductively coupled plasma etcher (ICP), the nitride etch gave clear pattern transfer by etching all the way through the nitride, exposing the silicon substrate.

With the nitride removed, the silicon etch could be performed. This process used a wet etch with 30% potassium hydroxide (KOH). Due to the <100> orientation, the exposed silicon was etched at a 54.74° angle. Etch rates of 1 to 1.6 μm per minute were obtained with etch selectivity of nearly 1000:1, silicon to silicon nitride. After the nitride etch was completed, the thin free-standing membranes (Figure 6.2) on the front-side were ready for patterning using electron-beam lithography. A drawback of this system is the proximity effect (broadening of the initial beam diameter and exposure of unwanted areas caused by electron-solid interactions). The proximity effect can be caused by both the forward scattering and the back scattering of electrons. Forward scattering – the small angle scattering experienced by electrons as they enter the resist – can be minimized by using the thinnest resist possible. In this method, the thickness of the resist was under 50

nm. Back scattering – the large angle scattering experienced by electrons as they pass through resist and enter substrate – can expose unpatterned resist. The electrons may return back into the resist at a significant distance from the incident beam, thereby blurring the desired patterns. This drawback of the back scattered electrons was nearly eliminated by using the thin free-standing membranes (Figure 6.2).

The wafer was selectively etched away to leave a layer of silicon nitride with a thickness of a few hundred nanometers. The e-beam pattern was then written on the membranes. The e-beam resist (2% 950K PMMA) was spun to 47-49 nm. E-beam exposure was performed with 2 nA current, 10 nm beam diameter, and 100 kV accelerating voltage. A lift-off process was performed using 20 nm gold with 5 nm chromium adhesion layer, and the sample was ready for characterization. The entire fabrication process is illustrated in Figure 6.2.

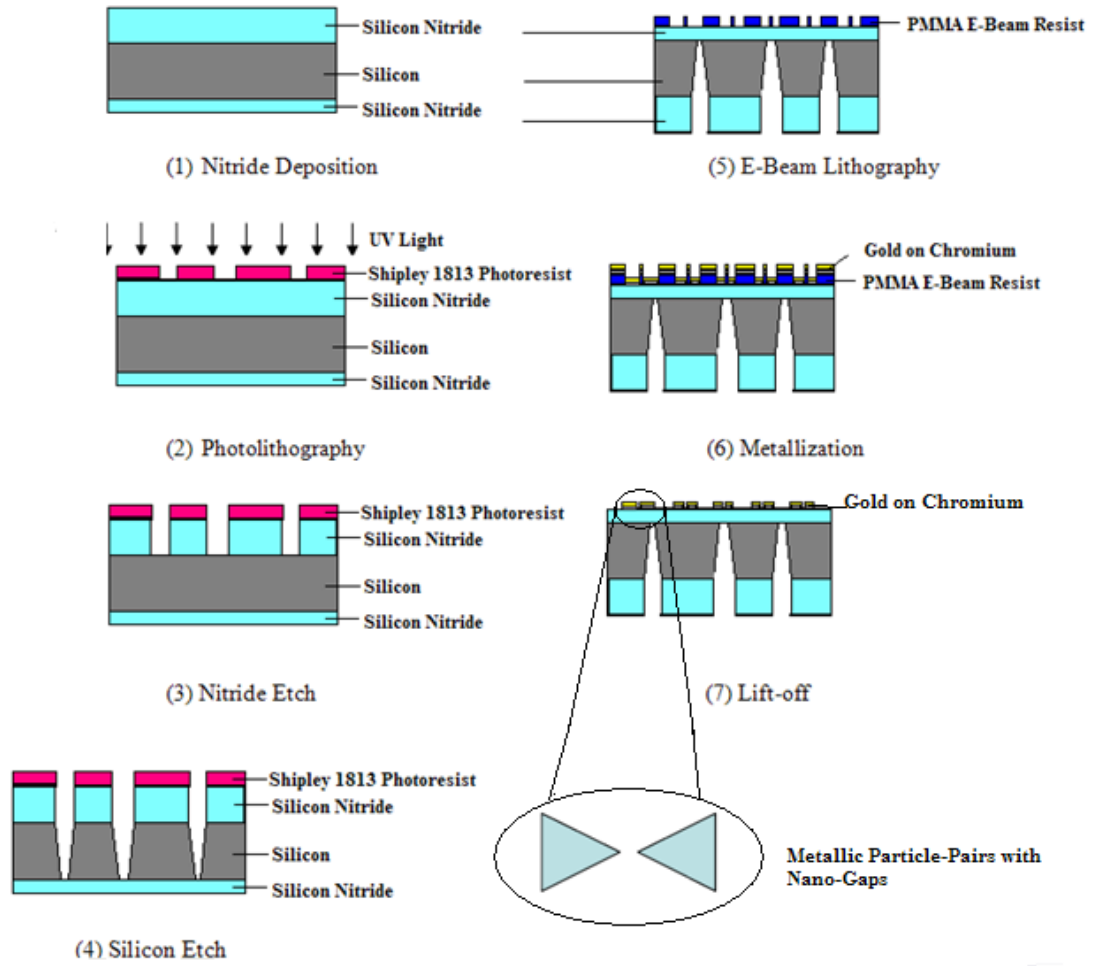


Figure 6.2: Fabrication process of metallic particle-pairs with nano-gaps on Si_3N_4 . (1) Silicon nitride is deposited on the wafer. (2) Photolithography is performed to create windows for subsequent etching. (3) Silicon nitride is etched. (4) Silicon wafer is also etched through. (5) Electron-beam lithography is performed to pattern the bow-tie structures with nano-gaps. (6-7) Metallization and lift-off generates metallic particle-pairs.

6.2.2 Method 2: Quartz Substrate [76]

The process-flow for nano-gap fabrication is as follows:

1. **Wafer Specifications:** Oxide/quartz wafer
2. **Resist Spin:** 80 nm 950K PMMA
3. **Electron Beam Lithography:** JEOL JBX-9300FS system with spot size of 14 nm and beam current of 2 nA
4. **Develop:** 1:3 MIBK/IPA (10 s)
5. **Metallization:** Cr + Au (25 nm) in high-vacuum e-beam evaporator
6. **Lift-off:** n-methyl-pyrrolidone at room temperature

The e-beam lithography system used a beam current of 2 nA with a spot size of 14 nm. Different process conditions were tested to identify the optimal develop conditions for sub-20nm gaps. Three different developers, 1:1 MIBK/IPA for 60s (developer A), 1:3 MIBK/IPA for 10s (developer B), and 7:3 IPA/DI water for 30s (developer C) were tested. For the lift-off, both hot (85 °C) and room-temperature n-methyl-pyrrolidone were tested. The dose ranged from 50 $\mu\text{C}/\text{cm}^2$ to 150 $\mu\text{C}/\text{cm}^2$ to identify the optimal dose (100 $\mu\text{C}/\text{cm}^2$). Developers A and C yield shapes that are not very sharp at the edges and this would result in a reduced enhancement of the surface-field for SERS. Developer B yields a good pattern as well as reproducible gaps. Also, room-temperature lift-off worked just as well as a lift-off at elevated temperatures.

The optimized process conditions resulted in sub-20 nm gaps with good repeatability. Detection of SERS not only requires small gaps but also uniform ones (i.e. with a low deviation from the mean gap value). Both the develop and the lift-off processes did not have much of an impact on gap-uniformity. It was found that the way the pattern file was designed had a big influence on gap-uniformity. Some machine writing strategies may optimize intra-field patterning and this might actually deteriorate the gap distribution. An example of this is when left-pointing particles are written first followed by all the right-pointing ones (assuming the pattern consists of particle-pairs as shown in Figure 6.1). The pattern file was designed such that the machine was forced to write both particles in a pair one after the other. Such a pattern design greatly improved the uniformity of nano-gaps fabricated in this work.

To achieve a narrow gap distribution, another important factor to consider is shot pitch. Shot pitch is dependent on a number of different parameters – the maximum deflector frequency (f_{def}), beam current, and dose. For the results reported in this work, f_{def} is 50 MHz. This places a lower limit on the achievable shot pitch (2 nm in this case). Since the process reported here uses a diluted developer and a short develop time, high doses are needed to pattern nano-gaps.

When patterning on insulating substrates, such as quartz, an anti-charge layer would need to be used. Two types of anti-charge layers were experimented with – a 5 nm layer of Au, and ESPACER (a water-soluble polythiophene derivative) [77]. Both of these approaches proved effective in achieving well-defined patterns. Au deposition was done in a filament-evaporator; this process step takes a considerable amount of time since it is done in vacuum. A quicker approach is to use the ESPACER. This water-soluble compound is spin-coated on the e-beam resist; after e-beam lithography and before resist develop, the ESPACER is washed away with water.

6.3 Results and Discussion

Method 1:

The process for fabrication of the nitride membranes was established and optimized. The membrane squares could be fabricated with a high yield per wafer. The yield per wafer for the membrane squares was 90%. The process worked very well and success was achieved for every trial using the double side polished wafers.

Characterization was performed using the Zeiss Ultra60 scanning electron microscope (SEM) and the Veeco Dimension 3100 atomic force microscope (AFM). The

AFM did not provide the resolution needed. Using the SEM, successful fabrication of nanometer-scale gaps was demonstrated. The smallest gap achieved using this method was 5.78 nm, as shown in Figure 6.3. By varying the dosage applied, the gap size varied until a point was reached when the dosage was too high and the pattern merged.

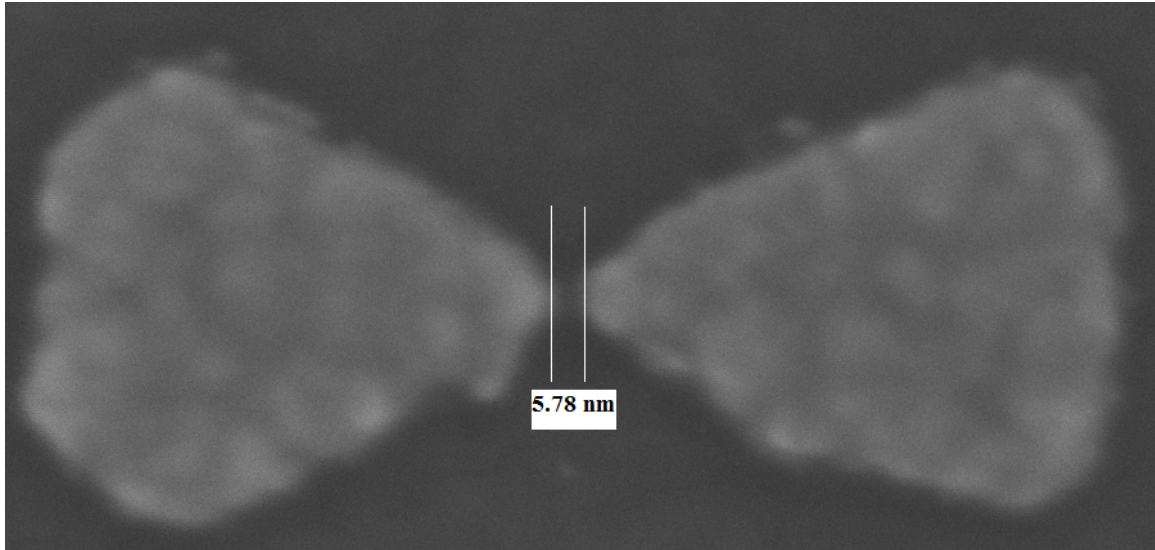


Figure 6.3: A 5.78 nm gap between the gold electrodes using 15 kV accelerating voltage and 2 mm working distance in the SEM.

While the gap sizes achieved were good, the most compelling results can be seen in Figure 6.4. These SEM images were taken right at the border of where the free-standing nitride membrane and the substrate-backed membrane patterns met. Step 7 of Figure 6.2 shows the cross-section of such a structure. Adjacent metallic particle-pairs may be sitting either on the free-standing nitride membrane region, or on the substrate-backed region. A clear distinction is seen between the patterns made on the substrate-backed nitride and the free-standing membranes (Figure 6.4). The patterns that were

written on the substrate were merged at a much lower dose due to backscattering of electrons inherent to e-beam lithography. The patterns were also skewed and tilted. On the other hand, the patterns that were written on the membrane came out very clear. The membranes produced smaller gaps with much greater precision, hence demonstrating that the problem of back scattering is significantly reduced in the free-standing nitride membranes.

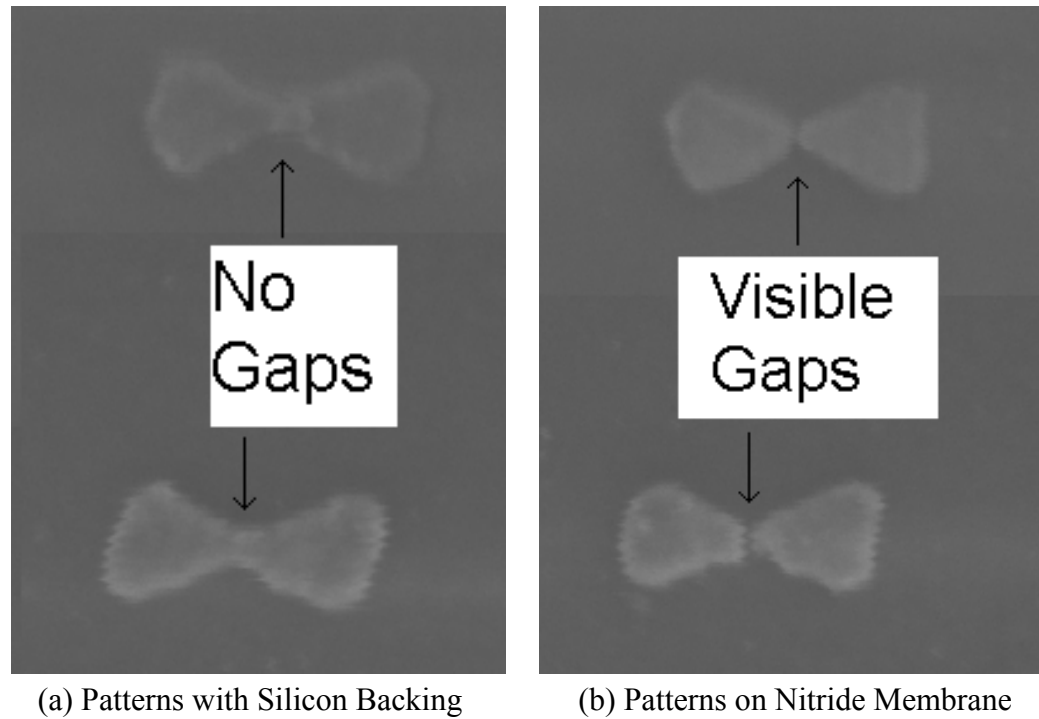


Figure 6.4: Comparison of patterns on (a) nitride membrane that is on top of the silicon substrate, and (b) nitride membrane that is free-standing.

The metal bow-tie structures on the Si_3N_4 substrate did not exhibit LSPR (Localized Surface Plasmon Resonance described in Section 6.1), hence no absorption spectra and SERS were achieved – a requirement for single-molecule detection. A transparent substrate is necessary for SERS; therefore, a quartz substrate was used for subsequent runs.

Method 2:

SEM imaging was carried out on the samples using a high-resolution Zeiss Ultra60 SEM which has an imaging resolution better than 2 nm at 1 kV. Low-voltage imaging becomes important for non-conducting samples. Figure 6.5 shows an SEM image of a particle-pair with a gap of less than 5 nm; the measured radius of curvature of the corners is less than 15 nm. Gaps smaller than this were obtained but could not be reliably measured because of limitations of the SEM. The smallest gap ever detected in these experimentations was 2.20 nm (Figure 6.6).

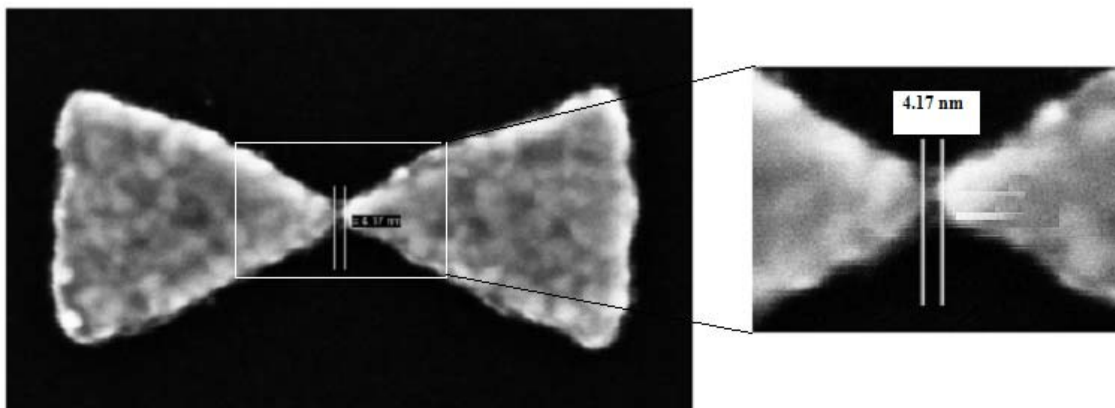


Figure 6.5: A 4.17 nm gap between the gold electrodes using 15 kV accelerating voltage and 2 mm working distance in the SEM.

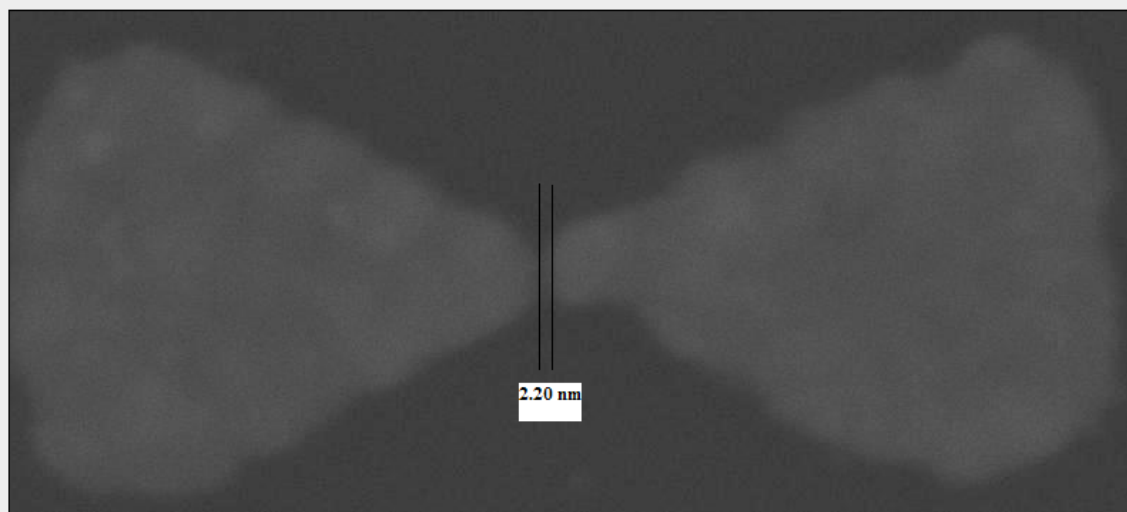


Figure 6.6: A 2.20 nm gap between the gold electrodes using 15 kV accelerating voltage and 2 mm working distance in the SEM.

Gap distribution was measured by sampling gap dimensions across the 300 μm x 300 μm pattern [76]. Figure 6.7 shows the gap distribution for a 17 nm gap. The standard deviation is found to be 5.4 nm, which is within the range to enable SERS detection.

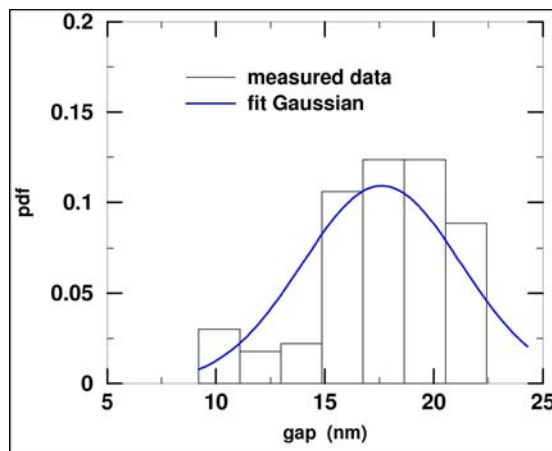


Figure 6.7: Gap distribution histogram along with a fit Gaussian curve. The mean is 17.6 nm and the standard deviation is 5.4 nm.

Table 6.1 shows the gap distribution for various mean gap-sizes. It can be seen that as the gap size decreases, the standard deviation slightly increases due to which the mean to standard deviation ratio increases to more than 73% for 9 nm gaps. In the reported process, the lower limit for a usable gap distribution is around 10 nm.

Table 6.1: Gap distribution for various mean gap sizes [76].

Mean Gap – μ (nm)	Absolute Standard Deviation – σ (nm)	σ/μ
8.9	6.5	0.73
11.2	6.4	0.57
13.1	6.2	0.47
17.6	5.4	0.31
21.6	4.5	0.21

6.4 Summary

This chapter listed several methods for the fabrication of sub-10 nm gaps between metallic particle-pairs. It demonstrated the use of the most reproducible method, electron-beam lithography, in fabricating nano-gaps between metallic bow-tie structures. Various e-beam parameters, such as shot pitch and beam interference, and process conditions, such as develop and lift-off conditions, were optimized for generation of nano-gaps with good repeatability.

The fabrication details of two methods of nano-gap patterning were illustrated. First, free-standing silicon nitride membranes were used which significantly reduced the

detrimental overexposure caused by back scattering of electrons. By this method, the smallest gap measured was 5.78 nm. Second, quartz wafers necessary for SERS were used. By this method, uniform sub-20 nm gaps useful for single-molecule detection were obtained. For a 17 nm gap, the standard deviation was found to be 5.4 nm. The lower limit for a gap distribution usable for SERS was around 10 nm. The smallest gap measured was 2.20 nm. The successful fabrication of a nano-gap between two nano-structures provides a strong mechanism for the development of innovative nano-electronic device structures.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The primary objective of the current research has been to fabricate high-mobility selective epitaxial graphene. The fabrication-toolkit consisting of selective epitaxial graphitization (Chapter 2) and nano-gap fabrication (Chapter 6) form building blocks for potential novel device architectures.

- AlN deposited by MBE acts as an effective mask against subsequent graphitization. By selective capping of SiC with AlN, electronic-quality graphene is epitaxially grown in desired regions.
- Temperature, growth-time and background argon pressure were critical process parameters. A delicate balance had to be reached to promote graphitization and prevent AlN degradation.
- AlN etching has been optimized to open up windows to the SiC for graphene-growth. No visible etch-residues are present.
- The highest Hall mobility of selective epitaxial graphene measured has been $\sim 1550 \text{ cm}^2/\text{Vs}$. Significant disorder within the graphene limits its mobility.

7.2 Key Contributions

- Epitaxial graphene is successfully grown on selected regions of SiC not capped by AlN deposited by molecular beam epitaxy. This contribution enables the formation of *electronic-quality graphene in desired patterns* without the need for

etching and any detrimental contact with external chemicals [34]. Raman analysis proves that SiC regions capped by AlN resist graphitization, while uncapped regions do not (Figure 7.1).

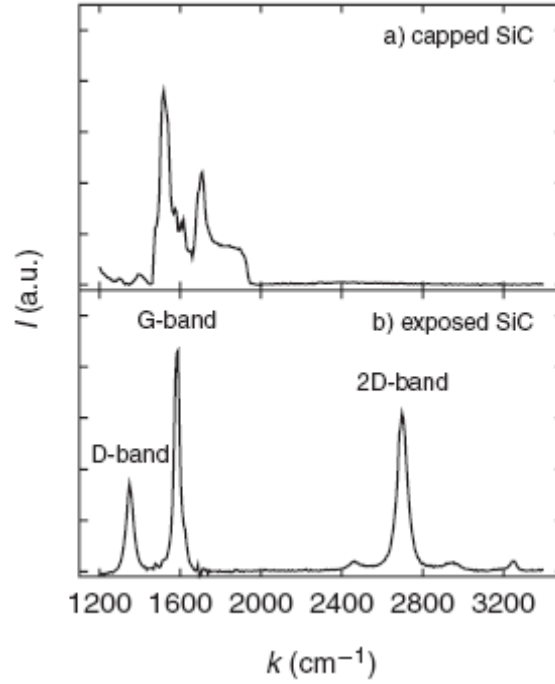


Figure 7.1: Raman spectroscopy of SiC: a) Capped with AlN, b) Exposed SiC.

- ***Etching of AlN in desirable patterns for selective graphitization without leaving etch-residues has been optimized*** for the purposes of this specific process of selective graphitization. Wet etching of AlN leaves residues on the SiC surface, leading to a surface roughness value of about 10 nm (Figure 7.2). A dry etching method was implemented that significantly reduced the roughness value to 1.5 nm (Figure 7.3).

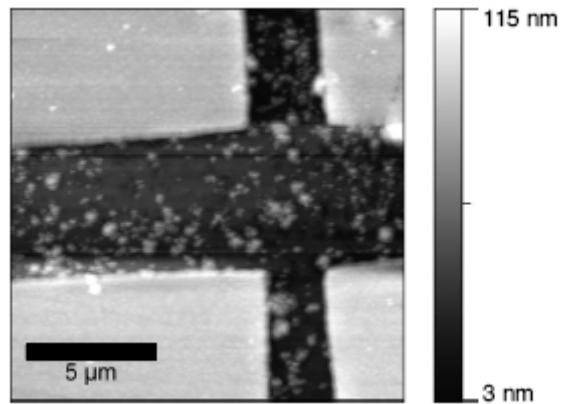


Figure 7.2: Wet-etching with surface roughness of 10 nm. AlN etch-residues are clearly visible in the patterned region.

Optimized AlN Etch:

- **Machine:** Plasmatherm ICP etch-system
- **Gas Flow:** Cl_2 (32 sccm), BCl_3 (4 sccm), and Ar (5 sccm)
- **Power:** 500 W (Coil); 70 W (Platen)
- **Pressure:** 5E-3 Torr
- **DC Bias:** 250-275 V
- **Time:** 60 s

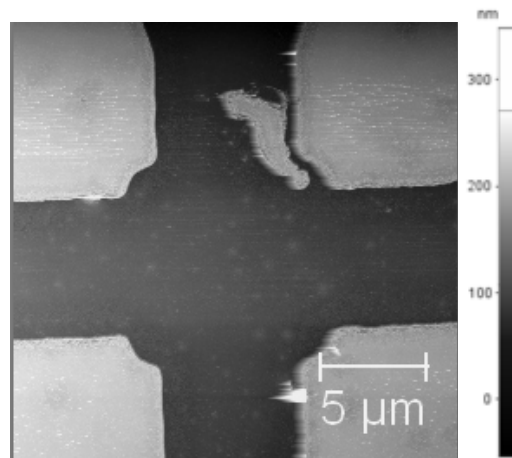


Figure 7.3: Dry-etching with surface roughness of 1.5 nm. AlN etch-residues are not visible.

- The *impact of process parameters (argon pressure, temperature, and time during graphitization) on the growth of graphene is characterized* [78]. A delicate balance between temperature and pressure is found to be essential during graphitization with the following behavior:

- **Temperature > 1400°C** leads to massive AlN deterioration

Temperature < 1400°C affects graphene-quality

- **Pressure > 50 mbar** hinders graphene growth

Pressure < 1 mbar leads to massive AlN decomposition

Optimal Growth Conditions for Selective Graphitization on C-Face:

- Temperature (1400°C)
- Pressure (1 mbar)
- Time (20 min)

- *First-ever electronic transport measurements are achieved* on the selective epitaxial graphene. After the first pioneering investigations of selective graphitization of SiC via AlN capping, Hall mobility of about 600 cm²/Vs was obtained [34]. A 5 μm x 100 μm Hall-bar was used to perform electronic transport with the following transport results:

Transport Results:

- ❑ Sheet Resistance: 1kΩ/□
- ❑ Electron Density: 1.08 x 10¹³ cm⁻²
- ❑ Hall Mobility: ~ 600 cm²/Vs

Since then, great strides have been made in optimizing the growth-process [79] by adding an extra masking layer of SiO₂ on top of AlN, and by residue-free AlN etching. With these enhanced processing techniques, a 5 μm x 70 μm Hall-bar was used for electronic transport with the following improved results. An increased Hall mobility of $\sim 1550 \text{ cm}^2/\text{Vs}$ was obtained.

Improved Transport Results:

- ❑ Sheet Resistance: $0.9 \text{ k}\Omega/\square$
- ❑ Electron Density: $4.12 \times 10^{12} \text{ cm}^{-2}$
- ❑ Hall Mobility: $\sim 1500 \text{ cm}^2/\text{Vs}$
- ***Topographical characterization of selective graphene*** was performed using AFM (Figure 7.4) and Raman (Figure 7.5).

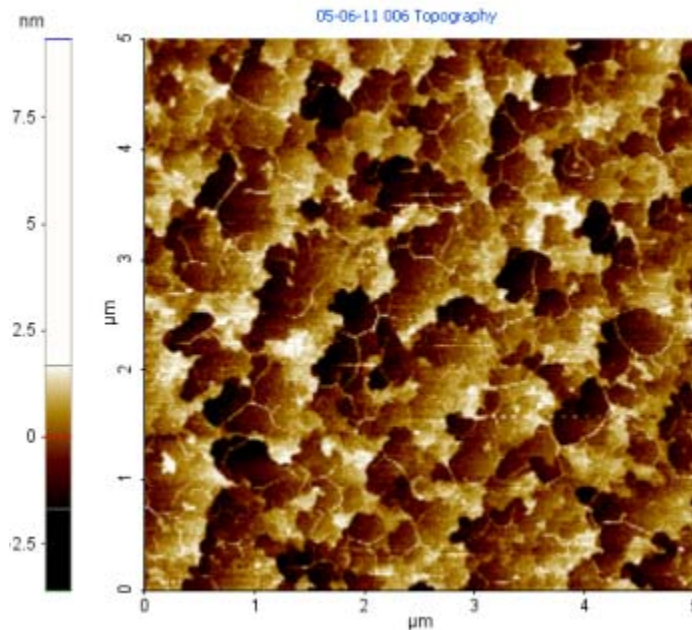


Figure 7.4: AFM of selective epitaxial graphene grown under optimal conditions. Graphene pleats are apparent.

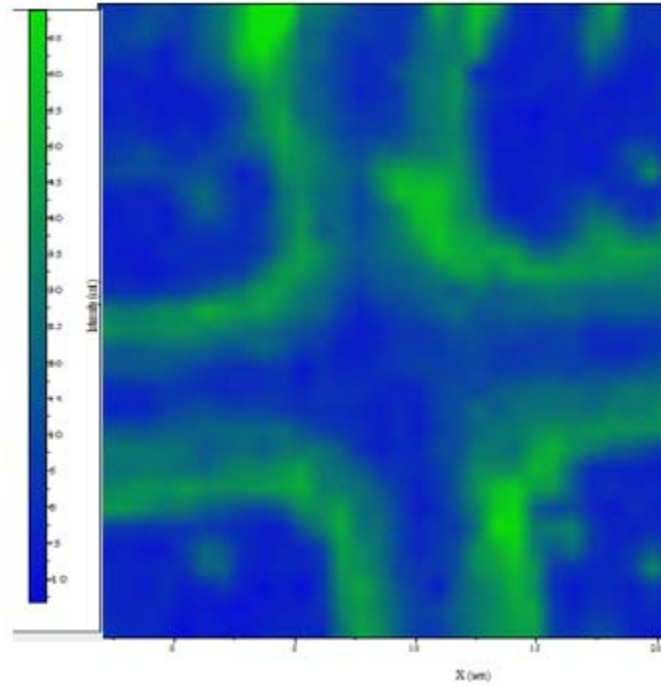


Figure 7.5: Raman 2D intensity of part of graphene Hall-bar. Graphitization starts to occur first along the AlN boundary closest to the area from which AlN is etched away.

Such surface-characterization shows that preferential graphitization of SiC along the AlN boundary occurs during the process of selective graphitization using AlN capping-layer (Figure 7.5). Also, the graphene thus grown shows numerous pleats (Figure 7.4), which potentially inhibit mobility. Large D-peak (Figure 7.1) also reduce mobility. Other limitations of the selective epitaxial graphene growth have been understood (Section 4.1) with potential methods of improvement put forth (Section 4.3).

- ***Challenges to the implementation of an RF FET*** using selective graphitization process are detailed in Section 5.4. Using the innovative technique of selective graphene growth, Hall mobility ($>1000 \text{ cm}^2/\text{Vs}$) comparable to that formed in current state-of-the-art graphene RF FETs has been demonstrated. Higher mobility translates to higher cutoff frequency and improved RF FET performance.

- Bow-tie nanostructures with *sub-20 nm gaps have been reproducibly obtained* [76]. One such structure with a sub-5 nm gap is shown in Figure 7.6, with 2.20 nm being the smallest gap observed with SEM. A uniform array of metallic particle-pairs with nano-gaps has viable applications in single-molecule detection.

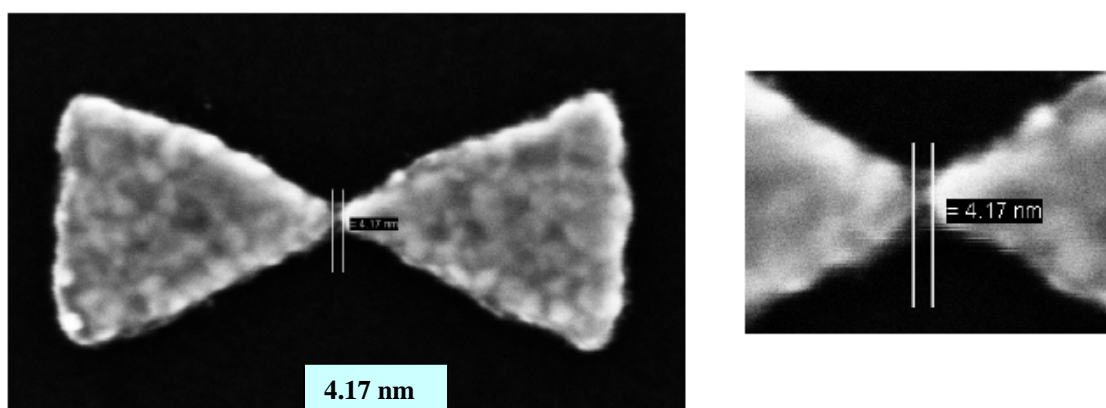


Figure 7.6: SEM image of a sub-5 nm gap between gold particle-pairs.

7.3 Recommendations for Future Work

- Optimal control of the argon pressure to enable controlled growth of graphene directly under the AlN will pave the way for novel device architectures with fewer fabrication steps. The AlN can be used as the gate dielectric modulating the graphene channel under it. Under high vacuum, graphene was formed over the entire SiC surface irrespective of the AlN capping layer. On the other hand, use of atmospheric pressure of argon during the process totally inhibited growth. In an intermediate Ar pressure of ~ 1 mbar, graphene was formed predominantly in the regions uncapped by AlN. However, certain areas of AlN were still affected with graphene growing under it. This proves that the Ar pressure during growth is an important parameter for the selectivity of the graphitization process. Fine tuning it

could therefore provide a pathway towards encapsulating graphene under a dielectric (in this case AlN with a bandgap of 6.2 eV [54]) without intermediate atmospheric contact. AlN is a good dielectric due to its large bandgap. Thickness control is critical for gate insulator, and AlN thickness remains essentially unchanged post-graphitization.

- With effective capping layer (such as BN on top of AlN), graphitization can occur at higher pressure and temperature which is more conducive to greater domain size and mobility on the C-face. The high-mobility graphene material can in turn usher in high-speed devices, as described in Chapter 5.
- With a high-mobility graphene channel in place, high-k dielectric capabilities need to also be put into effect to prevent gate tunneling current and preserve the mobility in an RF FET implementation.
- So far, topological-characterization has been performed using AFM and Raman spectroscopy. With improved surface-morphology possibly by implementing the recommendations listed in Section 4.3, scanning tunneling microscopy (STM) could be performed to gain more insight into the structure of the selective graphene. XRD could also shed light into the crystallinity of graphene grown in this manner.
- As the process of selective graphitization is further optimized resulting in high-mobility graphene-growth without deterioration of the masking-layer, it would be useful to investigate the impact on mobility of reduced channel length dimensions.

- Consequently, it would also be insightful to compare mobility of graphene grown by the process of selective graphitization, to that of etched graphene. Etched graphene refers to the typical method of growing graphene [21]. This means that SiC is graphitized without any masking-layer, and lithography is performed to pattern the Hall-bar onto the graphene by etching away the graphene from undesired regions. By making such a comparison, the effect of graphene-contact with extraneous chemicals can be better understood.
- As the selective graphitization of SiC is more precisely controlled, electronic-quality homogeneous graphene films can be more reliably produced. With greater process control, the edge-termination of the graphene nano-ribbon could potentially be desirably tuned. This in turn could lead to seamless device integration using all-graphene components based on the orientation of the edge-termination. Metallic and semiconducting properties can be obtained by zigzag and armchair ribbons respectively, enabling all-graphene electronically coherent devices.

APPENDIX A

FABRICATION PROCESS-FLOW

This section gives the schematic for the fabrication process (outlined in Section 2.2) for graphitizing the SiC via AlN etching using two methods. First, resist is used as the etch-mask for AlN. In the second method, an additional SiO₂ layer is used as an etch-mask.

A.1 Resist as Etch Mask



Figure A.1a: Resist is spun on AlN to act as the etch mask.



Figure A.1b: Resist is exposed and developed to expose the AlN.

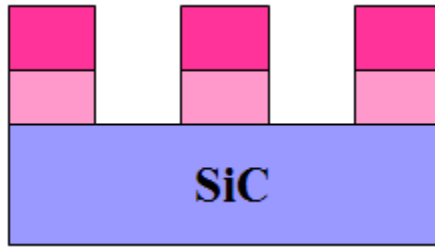


Figure A.1c: AlN is etched using resist as the etch mask.

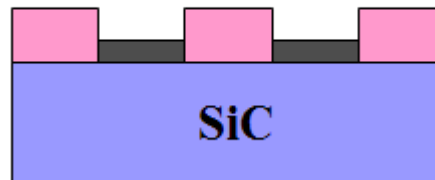


Figure A.1d: Exposed SiC regions are graphitized.

A.2 Silicon Dioxide as Etch Mask



Figure A.2a: Resist and silicon dioxide are spun on AlN to act as the dual etch mask on top of AlN.

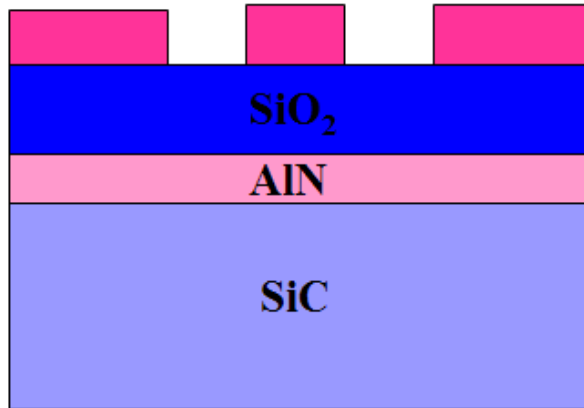


Figure A.2b: Resist is exposed and developed to expose the SiO₂.

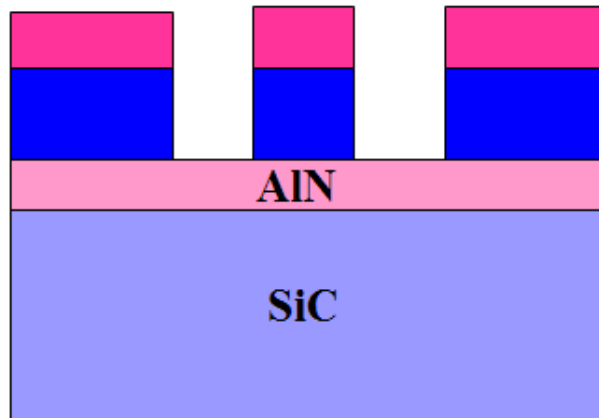


Figure A.2c: SiO₂ is etched using resist as the etch mask.

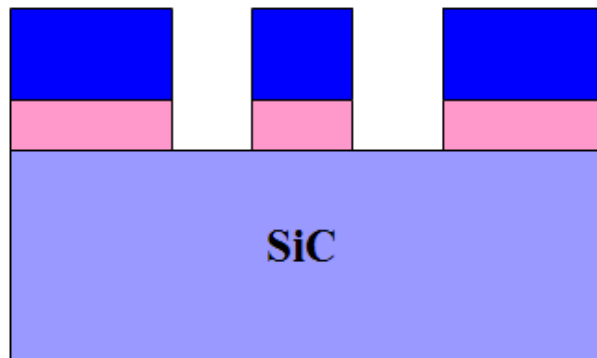


Figure A.2d: AlN is etched using SiO₂ as the more robust etch mask.

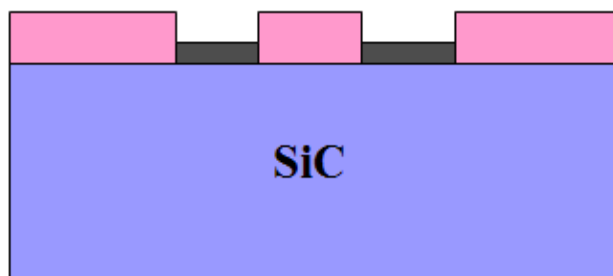


Figure A.2e: Exposed SiC regions are graphitized.

APPENDIX B

HYDROGEN-ETCHING RESULTS

Chapter 2 described the process-flow for selective growth of epitaxial graphene. Here are the details for the hydrogen-etching step:

B.1 SiC Substrate

Specifications:

- Semi-insulating
- 4H-SiC
- CMP C-Face & Epi-Ready Si-Face

Sample Preparation:

- Dicing: 1 cm x 1 cm
- Sonication-Clean: Acetone (10 min) and IPA (10 min) in dedicated pyrex beakers, followed by N₂ dry using teflon-coated tweezers

B.2 Hydrogen-Etching Process

Hydrogen-etching was performed in the FirstNano CVD Furnace in the Nanotechnology Research Center. The following process parameters gave the most optimal results for C-Face:

☐ **Gas Flow:**

H₂ (1000 sccm)

Ar (3800 sccm)

[Ratio = 26% H₂:74% Ar]

☐ **Temperature:** 1500°C

☐ **Pressure:** 4.325 Torr

☐ **Time:** 30 min

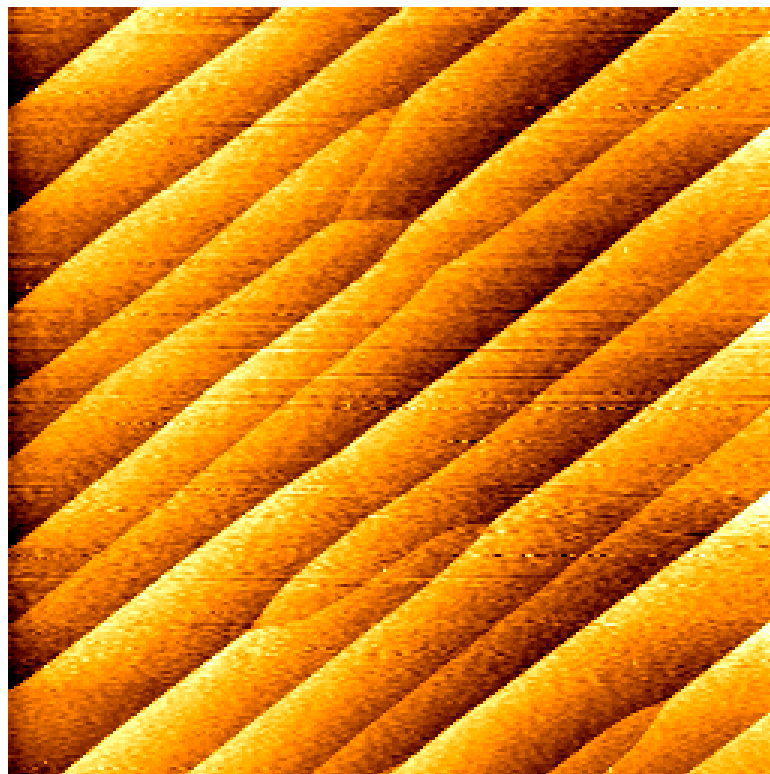


Figure B.1: AFM after hydrogen-etching (C-face; 20 μ m scan-size).

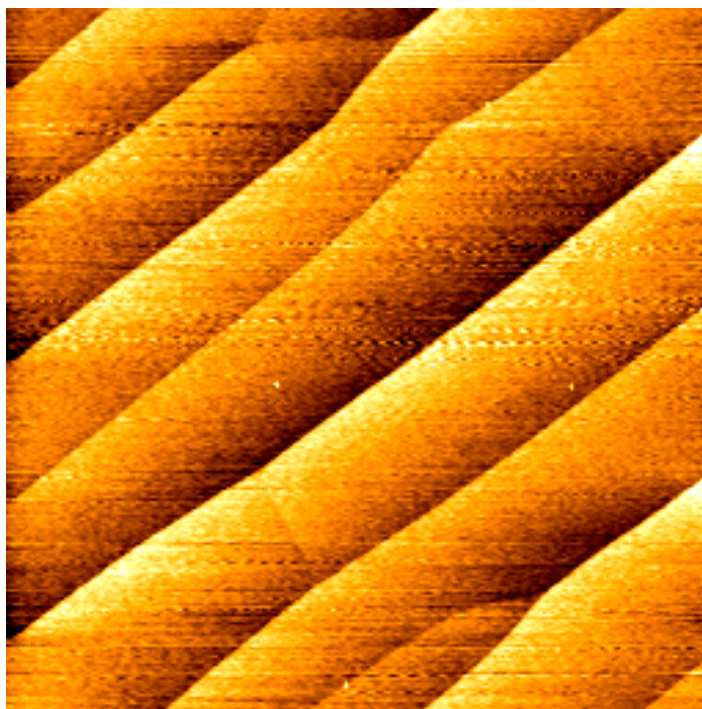


Figure B.2: AFM after hydrogen-etching (C-face; 10 μm scan-size).

Since C-Face has a different rate of etching than Si-Face, it needs a higher hydrogen flow-rate. The flow-rate was therefore reduced for Si-face, and the following conditions gave the most optimal results for hydrogen-etching for this polar face of SiC.

☐ **Gas Flow:**

H_2 (200 sccm)

Ar (3800 sccm)

[Ratio = 5% H_2 :95% Ar]

☐ **Temperature:** 1500°C

☐ **Pressure:** 4.2 Torr

☐ **Time:** 30 min

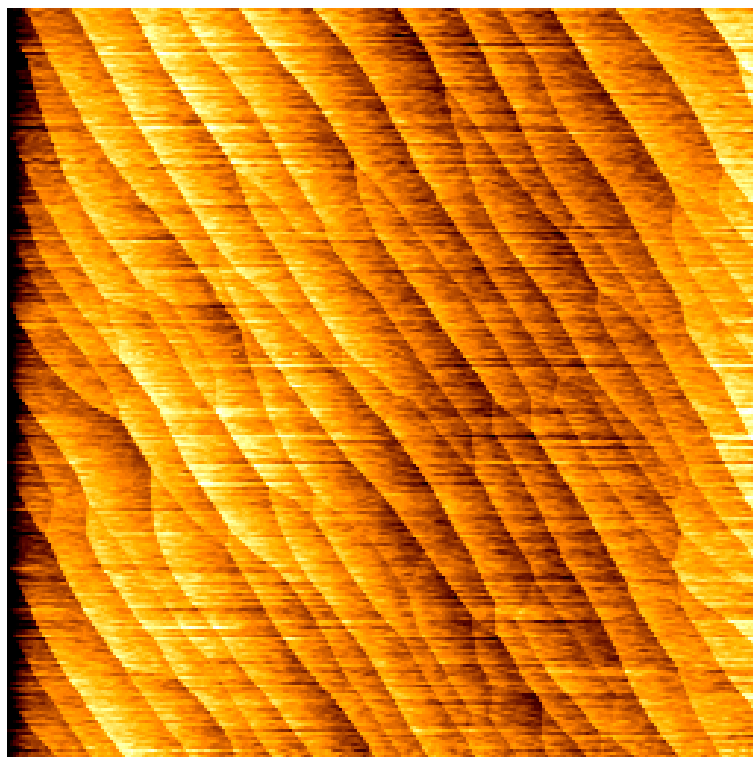


Figure B.3: AFM after hydrogen-etching (Si-face; 20 μm scan-size).

Under these same conditions, the C-face appeared as shown in Figures B.4 – B.5. The C-face shows 2 nm pits (measured by AFM) in the SiC after hydrogen-etching. For the purposes of this project, hydrogen-etching was performed on the C-face of SiC using the optimal conditions listed earlier.

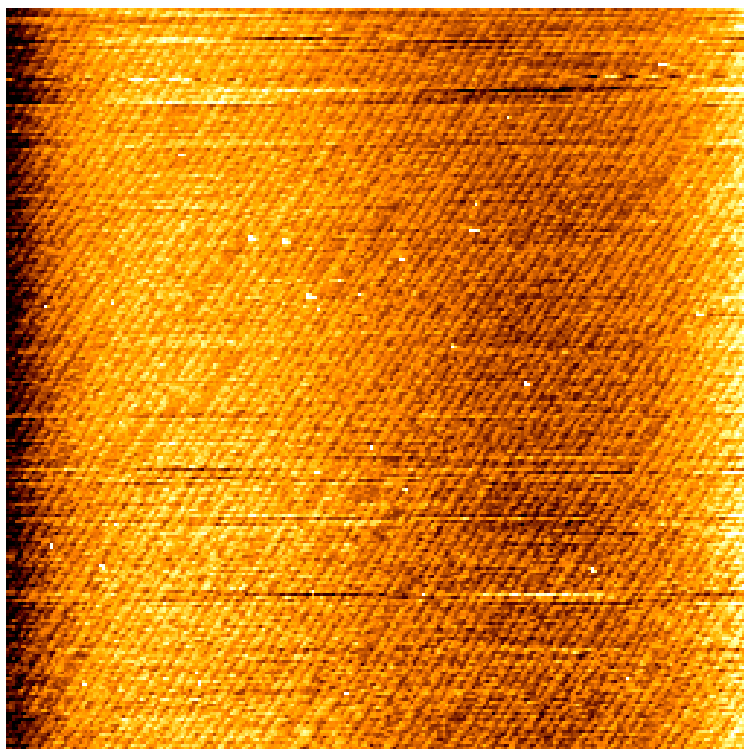


Figure B.4: AFM after hydrogen-etching (C-face; 20 um scan-size).

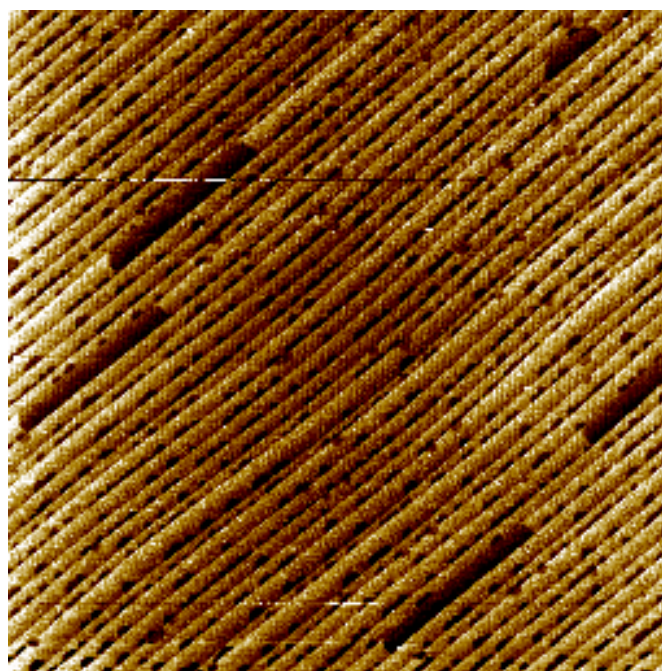


Figure B.5: AFM after hydrogen-etching (C-face; 10 um scan-size).

APPENDIX C

BASICS OF MOLECULAR BEAM EPITAXY

C.1 Molecular Beam Epitaxy (MBE)

Alfred Y. Cho at Bell Telephone Laboratories first used the term MBE in 1970 after extensive work on epitaxial films by several researchers, as described in [80, 81]. MBE is a technique for epitaxial growth via the interaction of one or several molecular or atomic beams on the surface of a heated crystalline substrate [82]. This interaction takes place in an ultra-high vacuum chamber ($\sim 10^{-9}$ torr). At this pressure the mean free path of a gas particle is approximately 40 km, promoting several collisions of the gas molecules with the chamber-walls before colliding with each other. The low background pressure also enables ultra-high purity of epitaxial films, reducing contaminants significantly compared to typical chemical vapor deposition conditions.

Figure C.1 is a schematic of a typical MBE system [82]. The chamber is cryogenically cooled with liquid nitrogen (LN_2), and the chamber walls prevent miscellaneous atoms from bouncing back from the chamber walls, thereby serving as a cryopump during growth. The group III-metal sources (such as AlN) and dopant materials are introduced through an effusion cell, where a solid material is placed in a crucible (typically made of pyrolytic boron nitride) and heated until the material sublimates or evaporates.

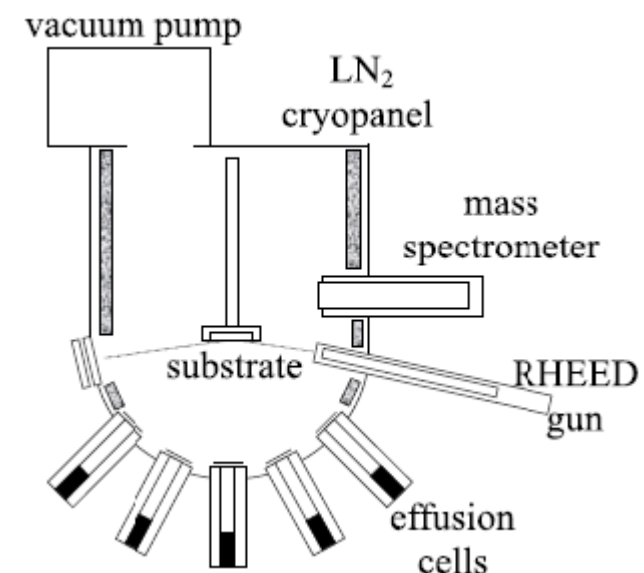


Figure C.1: Typical schematic of a MBE system [82].

The temperature of the effusion cells is controlled by proportional-integral-derivative (PID) control parameters, where the flux intensity can be maintained to within 1%. AlN films deposited for selective growth of graphene described in this dissertation use Al in the crucible and a nitrogen RF plasma source, where purified N_2 is converted into a more active atomic and molecular species. Shutters placed in front of the III-V sources allow direct control of the epitaxial growth surface at a monolayer level by changing the incoming beam with the opening and closing of the shutter.

C.2 Reflection High-Energy Electron Diffraction [83]

As mentioned previously, MBE systems maintain a base pressure less than 10^{-9} Torr. This base pressure allows for sophisticated *in-situ* growth analysis. Reflection high-energy electron diffraction (RHEED) is one such technique that was used during the MBE of AlN for this project. A RHEED system uses an electron gun that generates a

beam of electrons that strike the epitaxial surface at a small angle. The incident electrons diffract from the atoms on the surface, and a fraction of the diffracted electrons interfere constructively at specific angles to form regular patterns on the detector. The electrons interfere according to the position of the atoms on the sample surface, giving an indication of the growth surface.

RHEED analysis is only a surface technique, and is therefore not capable of determining bulk quality. Oscillations of the RHEED intensity (RHEED transients) can also provide information about the time needed to grow a monolayer of material. However, RHEED transients are rarely observed in the case of III-Nitrides because layer by layer growth does not normally occur. Burnham et al. [84] created a closed-loop system using the RHEED oscillations and shutter modulation to reliably reproduce quality AlN.

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VITA

FARHANA ZAMAN

Farhana Zaman was born one fine day in spring to loving parents, Mr. A.K.M. Khalequzzaman and Mrs. Nasreen Zaman. At six-months old she took her first plane-ride from her home-country of Bangladesh to the Arabian country of Kuwait. Her childhood days were spent relatively carefree, sheltered by her parents from the adversities of the world. Escaping as a refugee during the Gulf War of 1990 was a brief episode of anxiety and uncertainty. Fortunately, stability was restored and Farhana had a fulfilling early life. She learnt five languages in school – English, Bengali, Hindi, Arabic, and French.

Following high-school she traveled the distance between Kuwait to the United States in the quest of a college education. As an undergraduate in Electrical Engineering at Georgia Institute of Technology, she worked for the first time in her life as a coop in the Microelectronics Research Center. She got so interested in what she saw that she achieved the Best Coop of the Year Award, and went on to pursue her post-graduate studies in this specialization. Farhana was awarded the Graduate Woman's Fellowship for Leadership in Microelectronics by Texas Instruments, based on "her high grade point average, faculty endorsements, and her leadership and innovative research in nanogap fabrication." As a Graduate Research Assistant, she also performed interdisciplinary research with the School of Physics in the revolutionary field of graphene. Her time at Georgia Tech culminated in a Doctor of Philosophy degree in Electrical and Computer Engineering in 2012.

Farhana is committed to mentoring for educational programs. She looks forward to continuing to make science accessible to everyone through outreach activities. She is a member of IEEE, APS and Eta Kappa Nu. Next item in her agenda is to join her husband and start their newly married life together. She aspires for both a rewarding personal and professional life. With all the blessings that have been bestowed on her, she wishes to give back to society by technological advancements.